INTEGRATED THREE-AXIS ACCELEROMETERS WITH NANOMETER SCALE CAPACITIVE GAPS AND SIGNAL CONDITIONING INTERFACE IC

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INTEGRATED THREE-AXIS ACCELEROMETERS WITH NANOMETER SCALE CAPACITVE GAPS AND SIGNAL CONDITIONING INTERFACE IC

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To my parents and my loving family

To bloom one mum flower, an owl must have cried since last spring

To bloom one mum flower, a thunder must have roared with dark clouds

"Beside the mum flower" – Seo Jeong-ju (Korean poet)

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SUMMARY

Microelectromechanical Systems (MEMS) accelerometers have been widely adopted in many areas of consumer electronics, automotive, and industrial applications due to their small size, low power consumption and low-cost integration. As technology advances, newly-emerging applications such as wearables, Internet-of-Things (IoTs), and health informatics, call for the higher performance MEMS accelerometers that achieve both very low noise and extended operational bandwidth, which is challenging to satisfy using existing technologies.

This dissertation focuses on implementing multi-axis capacitive MEMS accelerometers with high dynamic range that sense acceleration in wide frequency range (> 10 kHz) with considerable accuracy (< 100 μg/√Hz) by utilizing high aspect ratio (>100:1) nano-gap (< 300 nm) microstructures. Such feature provides an increased electro-mechanical coupling that enables improved operational bandwidth while achieving low-noise without altering device geometry. Furthermore, the use of nano-gap enables adjustment of air-damping so that the quasi-static (i.e. non-resonant) accelerometers can be operated in low-pressure level (1~10 Torr) without instability issues. Doing so paves the path toward the single-chip sensor fusion by enabling integration of quasi-static accelerometer with gyroscopes in low-pressure environment on a common silicon substrate. Both in-plane and out-of-plane accelerometers are designed and fabricated using the HARPSS process, and interfaced with a switched-capacitor signal conditioning IC to characterize their performances. The measurement results showed the sensor can achieve operational bandwidth higher than 8.5 kHz, and noise levels of 221 μg/√Hz and 72 μg/√Hz

for in-plane and out-of-plane devices respectively. The figure-of-merit (FOM) defined as the ratio of device bandwidth over noise density for the presented designs are orders of magnitude higher than that of other commercially available MEMS accelerometers.

To realize sensing gap in the nanometer range, a dedicated fabrication process (i.e. HARPSS), which gap size is determined by the thickness of thermally grown sacrificial layer is used. However, using such process makes it difficult to implement shock stop, which requires smaller gap size than sense electrode to prevent excessive proof-mass movement under high levels of accelerations, as it requires an increased number of optical masks as well as fabrication steps. To resolve these issues, a novel sloped-electrode, which enables creating different effective gap sizes by simply adjusting its geometry, is proposed and consecutive measurements were performed to validate the effectiveness of the scheme.

The changing capacitance from sensor element is converted into an electrical signal using a low-noise switched-capacitor (SC) interface circuit. Correlated double sampling (CDS) technique is introduced to eliminate inherent flicker noise of the amplifier, which is the dominant noise source of the circuit, and an extensive analysis was conducted to suppress other noise sources and attain high capacitive resolution. Measurement results showed that the presented readout IC achieves more than 10 times better noise performances compared to the previous circuit that was used to interface MEMS accelerometer. Furthermore, to minimize the effect of capacitance mismatches in the MEMS accelerometer, a precision calibration circuit that employs a time-averaged charge-tuning technique was incorporated into the readout circuit, achieving a resolution level of sub-aF and a wide calibration range of 300 fF.

1. INTRODUCTION

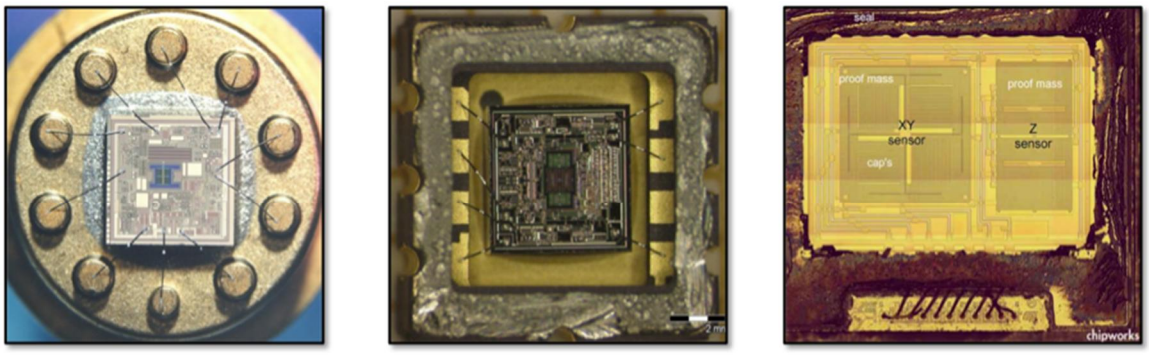
1.1. HISTORICAL PERSPECTIVE

The history of the accelerometer began in the year of 1923, when the American engineers Burton McCollum and his colleague Orville Peters published a paper called "New Electrical Telemeter" [1]. Their instrument had a pair of suspended resistor, which constitutes a half Wheatstone bridge and moves freely with respect to the external force so that its output voltage changes with respect to the applied acceleration. Still the size of the sensor was as large as cubic foot, limiting its usage into very specific areas, such as bridge monitoring, dynamometers, or recording acceleration of the aircraft. After the initial invention, Edward Simmons from the Caltech and Arthur Ruge from the Massachusetts Institute of Technology proposed the concept of strained-gauge accelerometer [2]-[3], replacing heavy resistor with bendable metal foil so that smaller form-factor as well as improved sensitivity can be achieved. During 1940s, the piezoelectric material, which generates an electric charge in response to the applied mechanical stress, were introduced to create accelerometer, providing improved robustness and wide input range compared to the prior designs. At this stage, the weight has scaled down to less than 100 grams and the size smaller than few cubic centimeters. However, the usage was still limited to shock and vibration measurement due to expensive cost and relatively large device size [4].

It was the advent of micro-fabrication technology that truly expanded the accelerometer application into a greater extent. In 1970s, James Angell from the Stanford University proposed an idea that uses micromachining technologies to implement the accelerometer by bonding the silicon proof-mass using two glass wafers on each side [5].

Unlike predecessors, their design achieved the capability of batch-fabrication, which reduced the production cost drastically. In 1991, Analog devices finally released the world's first commercial MEMS accelerometer ADXL50 [6], which was used to create crash sensor in air-bag deployment systems. Their device surpassed existing mechanical crash sensors in terms of both cost and performance. Their huge success let MEMS accelerometer to be widely accepted in commercial applications. In 2006, Nintendo introduced their new gaming console, *Nintendo Wii*, which incorporated 3-axis accelerometer (LIS3L02AE) from STmicroelectronics to detect user's motion and to control the game. In 2007, Apple introduced *iPhone*, which also integrated 3-axis accelerometer (LIS302DL) from STmicroelectronics for gravity detection and image stabilization [7].

After 80 years of development since its initial invention, the accelerometer has finally evolved into a size less than a grain (~ few millimeters) and achieved extremely low resolution close to micro-gravity (g=9.8 m/sec^2) level. Their vast application now starts to encompass wearable devices, health monitoring, and IoTs (Internet of Things).



(a) (b) (c)

Figure 1. 1: History and evolution of the accelerometer; (a) ADXL50 – World's first commercial MEMS accelerometer (b) ADXL278 – 2-Axis accelerometer (c) LIS33DLF – 3-axis accelerometer used in iPhone 4

1.2. MEMS ACCELEROMETER EVOLUTION

Since the beginning of MEMS accelerometer, the size of the sensor has been constantly scaled down as it lowers the overall production cost and expands its capability to be integrated with broader applications. Figure 1. 2 shows some examples on how the commercial companies have scaled down their sensor sizes. As shown in Figure 1. 2(a) [8], Analog devices have shrunk their accelerometer die size more than 4 times since its initial release. Similar effort was also done on packaging perspective as shown on Figure 1. 2(b), where STmicroelectronics have stacked their circuit die on top of the wafer-level packaged MEMS sensor to reduce the planar area of the entire package (LIS3DLH). Furthermore, Bosch Sensortec have employed wafer-level-chip-scale-package (WLCSP) technology to drastically miniaturize the area for their accelerometer product (BMA355) as shown in Figure 1. 2(c) [9][10]. Instead of using conventional resin mold as in conventional IC packaging, their product placed the number of solder balls directly on top of the capping wafer to make direct interconnection with outer environment, achieving device area close to MEMS die itself (1.5 mm × 1.2 mm).

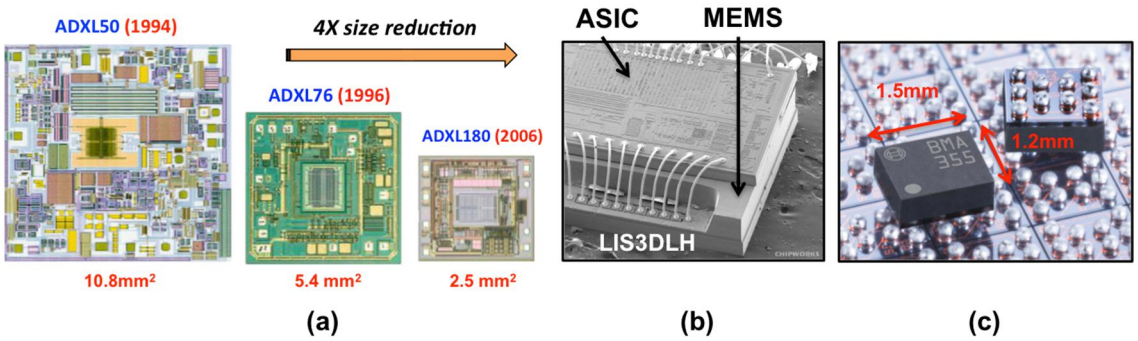


Figure 1. 2: (a) Scaling of accelerometer size from Analog devices [8] (b) SEM view of trial-axis accelerometer (LIS331DLH) using stacked die approach (C) Miniaturized accelerometer using WLCSP (BMA255) [9]

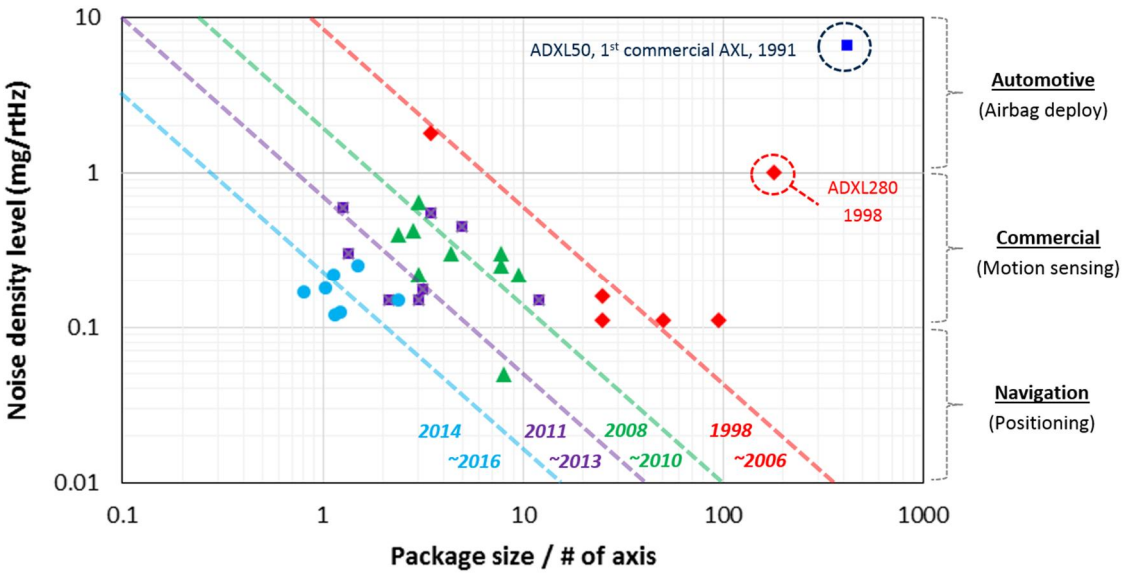


Figure 1. 3: Evolution of commercial MEMS accelerometer in terms of size and noise performance over the years [11]

Figure 1. 3 also plots the accelerometer size and its noise performances [11], clearly showing its continuous scaling toward miniaturization and low noise performance.

Another trend in the evolution of the MEMS accelerometer is the emergence of combo sensors (or Sensor-fusion), which integrates acceleration sensor with different devices, such as gyroscopes, or magnetometer, to attain multiple functionalities and to expand its application scopes toward the higher-end areas (e.g., inertial-navigation platform). Such shifts in the markets are clearly visible from Figure 1. 4 [14], where the portion of the stand-alone sensor (e.g. accelerometer, gyroscope, and magnetometer) is starting to face minor saturation after the year 2014. However, at the same time, the portion of 6- and 9-DOF (Degrees-Of-Freedom) sensors are booming rapidly and starting to dominate the entire inertial sensor market. Especially, by implementing an inertial-measurement-unit in single package, the device can be effectively used as personal navigation platform.

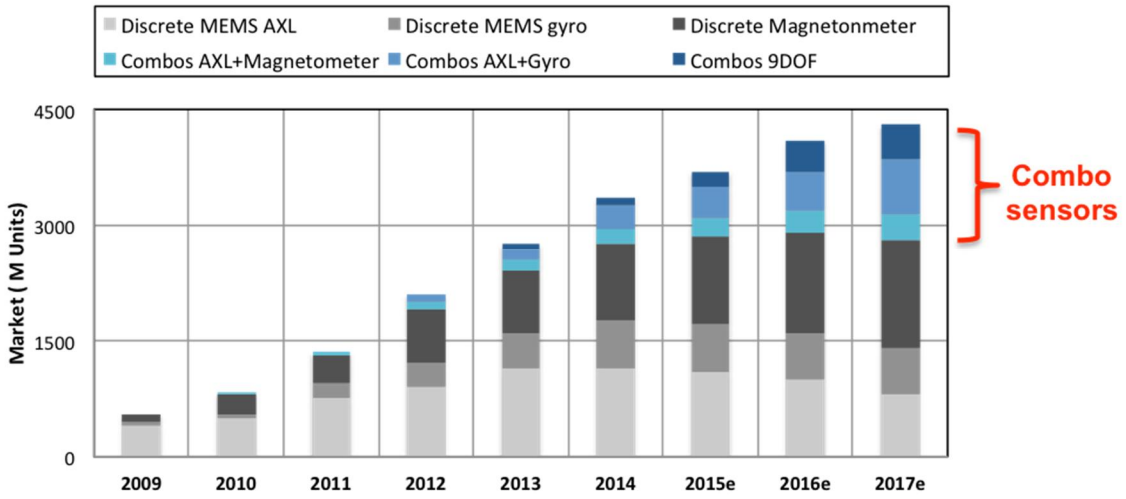


Figure 1. 4: Prediction of motion sensor for mobile phones and tablets - 2009-2017 market (M Units) [14] - Yole Dévelopment

Generally, these combo-sensors are manufactured by combining individual sensing elements using system-in-package (SiP) (Figure 1. 5) or by integrating multiple sensors on a single die as shown in Figure 1. 6. Each approach has its own pros and cons. Merging stand-alone sensors on a package may seem like a straightforward method, but has drawbacks such as increased production cost due to separate fabrication processes for each element, and the poor cross-axis sensitivity due to the misalignment during assembly process. These issues can be mitigated by integrating multiple sensors on a common silicon substrate as shown on Figure 1. 6. As the separate fabrication flows for each different sensors gets unified, the device would have better alignment as its alignment is done using optical lithography, which has orders of magnitude less error compared to traditional assembly process. However, complicated issues still exist due to fundamental differences between the operation of each sensors. The gyroscope is a resonant device, which requires a vacuum environment to minimize the air-damping and thereby attain high quality factor Q operation for better scale factor and lower noise. However, the accelerometer is a quasi-static device that needs to be operated under atmospheric level to have sufficient

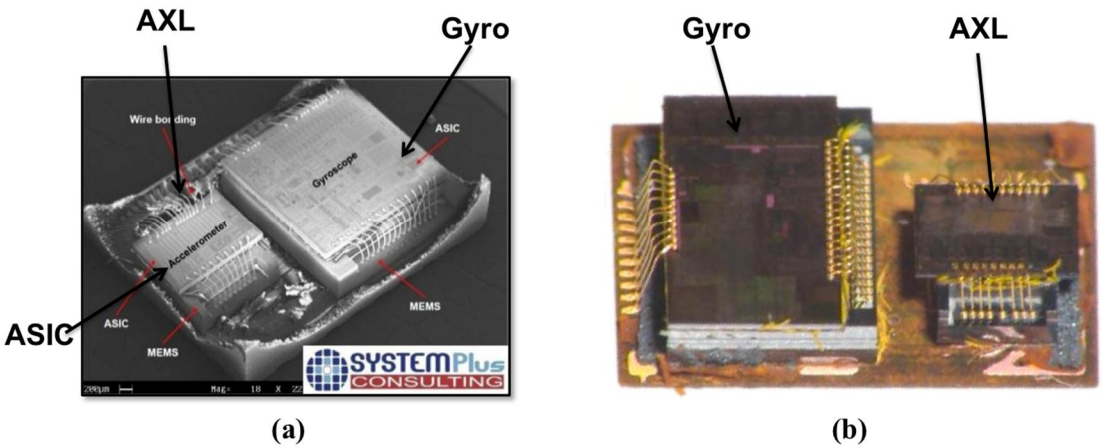


Figure 1. 5: Inside package view of 6-DOF sensor from (a) STMicroelectronics LSM330D and (b) Bosch Sensortec BMI055

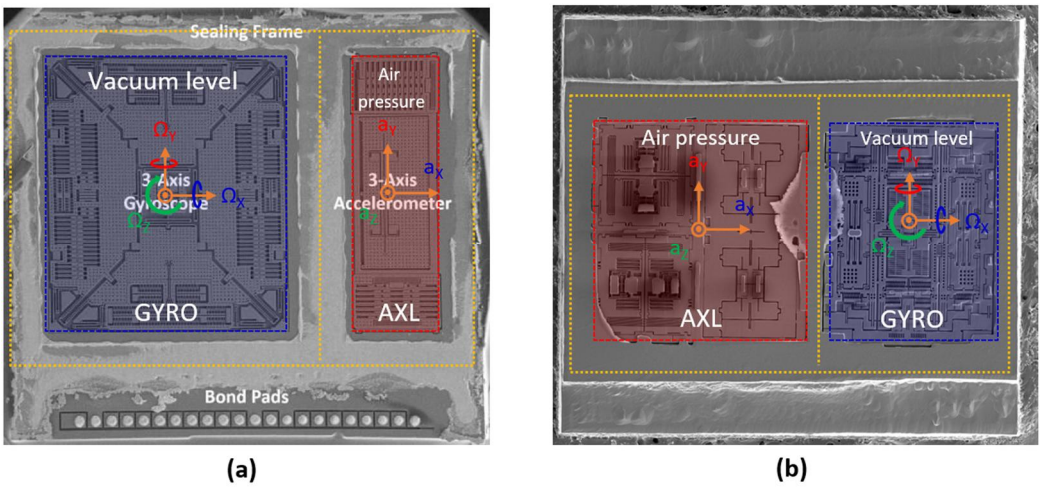


Figure 1. 6: Microphotograph of (a) STMicroelectronics LSM9DS0 and (b) Invensene MPU6050 after removing its capping wafer

air-damping and thus operated at critically-damped or over-damped condition. If the quasi-static accelerometer is operated with gyroscopes in same low-pressure level, the device would experience instability behaviors, such as long settling time and large overshoot as its operation gets under-damped. Due to such issues, commercial combo-sensors have separate wafer-level cavities so that each device can be operated under different pressure level. The tear-down microphotographs of the commercial 6-DOF sensors on Figure 1. 6 show that the accelerometer and the gyroscope are separated by the sealing frame to create

different pressure level cavities. The pressure levels between two regions are adjusted using getter [19], which traps the gaseous molecules by heating the metallic materials that is deposited inside the capping wafer. Still, doing so would increase overall production cost due to additional fabrication processes, and the pressure level created by the getter is not as good as sole vacuum-packaging process (i.e. large process variation). Table 1. 1 compares the performance between different combo sensors [20]-[24], which are implemented using separate-assembly and single-die integration process. As mentioned earlier, the devices implemented with single-die-integration have lesser size compared to that of the sensor manufactured using separate-assembly process.

Table 1. 1: Performance summary of multi-DOF sensors from commercial company

Model name	Implementation method	Package size	AXL noise	Type
STM – LSM330D [20]	Separate assembly	3 × 5.5 × 1.0 mm^3	220 µg/rtHz	3-axis AXL + 3-axis GYRO
Bosch Sensortec- BMI055 [21]		3 × 4.5 × 0.95 mm^3	150 µg/rtHz	
STM - LSM6DSM [22]	Single-die-integration	2.5 × 3 × 0.83 mm^3	130 µg/rtHz	
Invensense - ICM30630 [23]		3 × 3 × 0.98 mm^3	250 µg/rtHz	
Bosch Sensortec - BMI160 [24]		2.5 × 3.0 × 0.8 mm^3	180 µg/rtHz	

There is an increasing demand from newly-emerging technologies, such as wearables, IoTs (Internet of Things), and health informatics for the MEMS accelerometers having both wide operational bandwidth (> 10 kHz) and low-noise performance (<100 µg/√Hz), which are difficult to achieve using existing designs. This is clearly visible from Figure 1. 7, which plots the operational bandwidth and noise performance of MEMS

accelerometers that are developed from both academia and industry. It is interesting to note that their performances form a relatively straight line, commercial accelerometer having operational bandwidth in the range of 2 to 3 kHz and the noise level of 100 μg/√Hz, but the accelerometer from academia mainly focusing on achieving low-noise performance by sacrificing its bandwidth level. However, it should be strongly noted that there are no MEMS accelerometers available from academia and industry that provide both wide operational bandwidth and low-noise performance at the same time. So far, such performances can only be provided using non-MEMS piezoelectric accelerometers, which has size in the range of cubic centimeter, expensive cost, and AC-coupled output, meaning it cannot measure static accelerations [25]. Such characteristics makes the non-MEMS piezoelectric acceleration sensor not suitable for commercial applications.

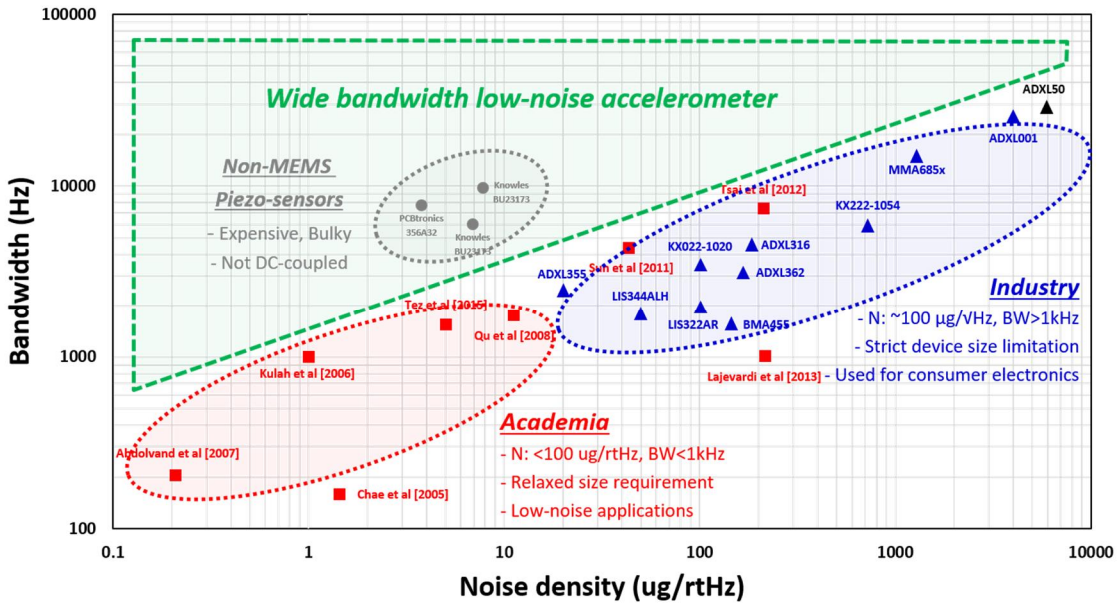


Figure 1. 7: List of MEMS accelerometers developed from both academia and industry with respect to operational bandwidth and noise density level

1.3. MOTIVATION AND OBJECTIVES

The motivation and objective of the following dissertation is to implement a multi-axis capacitive MEMS accelerometers platform with wide operational bandwidth (>10 kHz) as well as low-noise level (~100 μg√Hz). As it is challenging to attain such performances using current MEMS technology, designing an accelerometer, which meets the end goal of this dissertation, would open new possibilities for new applications. To achieve given task, we will be utilizing high aspect ratio nano-gap structure, which is orders of narrower than that of existing accelerometers. Doing so provides increased electromechanical coupling so that the accelerometer can have wide operational bandwidth without sacrificing its noise performance. Furthermore, use of nano-gap boosts the amount of air-damping so that quasi-static accelerometer can be operated at critically-damped or overdamped condition even under low-pressure level, thereby paving a way toward single-die-integration of inertial measurement unit (IMU).

Another objective of following dissertation is to implement precision readout circuitry that converts capacitance change caused by the acceleration into an electrical signal. The noise of interface circuit should be low enough to show the true performances of MEMS accelerometer. Moreover, the readout circuit needs to be capable of calibrate non-ideal capacitive mismatch and temperature variation from MEMS accelerometer, as it can lead to unwanted offset level and temperature induced drift. Considering that we are using nano-gap structure to implement accelerometer, non-idealities from the device would be even greater, and have significant effects on the system performance if it is not properly suppressed. To avoid such catastrophe, there is a urgent need for precision calibration block integrated inside the readout circuit.

This dissertation is organized as follows. **CHAPTER 1** introduces the history and evolution of MEMS accelerometers and the objective of this dissertation. In **CHAPTER 2**, design, fabrication and characterization of tri-axial nano-gap accelerometers achieving extended operational bandwidth will be discussed. **CHAPTER 3** describes on the design and the operation of readout circuit that is interfaced with the MEMS accelerometer, and proposes charge-tuning calibration technique to suppress capacitive mismatch. **CHAPTER 4** presents detailed analysis on the accelerometer interface circuit noise to determine major sources that effects on the performance, and to create precision readout circuit. Time-averaging operation is included inside the charge-tuning method to achieve extremely fine resolution level. **CHAPTER 5** shows the design of the single-proof-mass pendulum accelerometer, which provides multiple axis sensing under miniaturized device size. **CHAPTER 6** summarizes the overall dissertation followed by the future works.

2. NANO-GAP TRI-AXIAL MEMS ACCELEROMETERS

2.1. GENERAL OPERATION PRINCIPLE

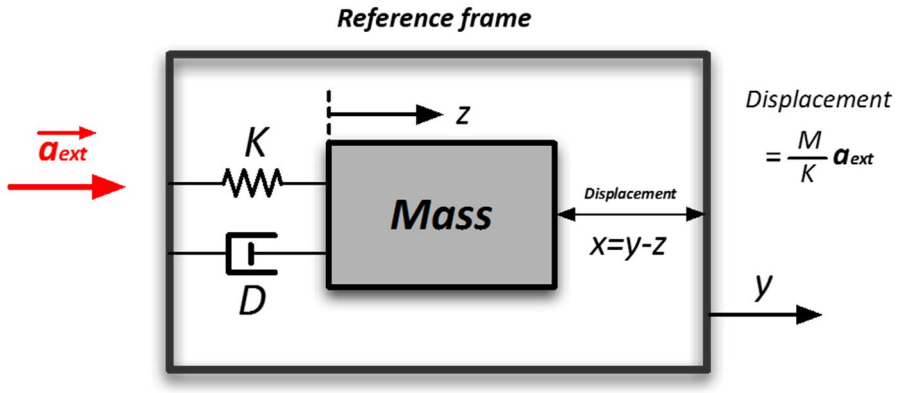


Figure 2. 1: Simplified lumped model of MEMS accelerometer

The general operation of accelerometer is explained using simplified lumped model in Figure 2. 1, which is consisted of the proof-mass (*M*) suspended to the reference frame via micro-mechanical spring (*K*) and damper (*D*). When external acceleration is applied, the reference frame moves toward the given direction (*y*), but the proof-mass tends to stay at the original position *(z)* due to its own inertia. This behavior results in displacement differences between the proof-mass and the reference frame, which is equivalent to *x=y-z*. The dynamic behavior of device movement is expressed using Newton's second law of motion (equation (2-1)). Assuming steady-state condition *($d^2x/dt^2=dx/dt\approx0$)*, the displacement is proportional to the applied acceleration as shown in equation (2-2).

$$M\frac{d^2x}{dt^2}+D\frac{dx}{dt}+Kx=F_{ext}=-M\overrightarrow{a_{ext}} \qquad (2\text{-}1)$$

$$x\approx\frac{M}{K}\overrightarrow{a_{ext}}=\frac{1}{\omega_0^2}\overrightarrow{a_{ext}} \qquad (2\text{-}2)$$

The transfer function between given external force F_{ext} and resulting proof-mass displacement x can be represented as equation (2-3). The MEMS accelerometer is a 2nd order spring-mass-damper system, which operational bandwidth is mostly determined by its resonant frequency ω_0. Therefore, if one wants to attain acceleration sensing capability over wide frequency range, the device needs to have high resonant frequency.

$$\frac{x(s)}{F_{ext}(s)} = \frac{1}{Ms^2 + Ds + K} = \frac{1/M}{s^2 + \omega_0/Q\, s + \omega_0^2} \qquad (2\text{-}3)$$

Depending on the transducing mechanisms of how the proof-mass movement is converted into an electrical signal, the accelerometer can be divided into three categories; piezoelectric [26]-[27], piezoresistive [28] and capacitive [29]. The capacitive accelerometer, which following dissertation will be mostly focusing, relies on a changing capacitance between proof-mass and sense electrode to detect external acceleration. As this type of sensing can achieve low-power operation, and can be easily implemented using silicon process, it is widely accepted to commercial accelerometers.

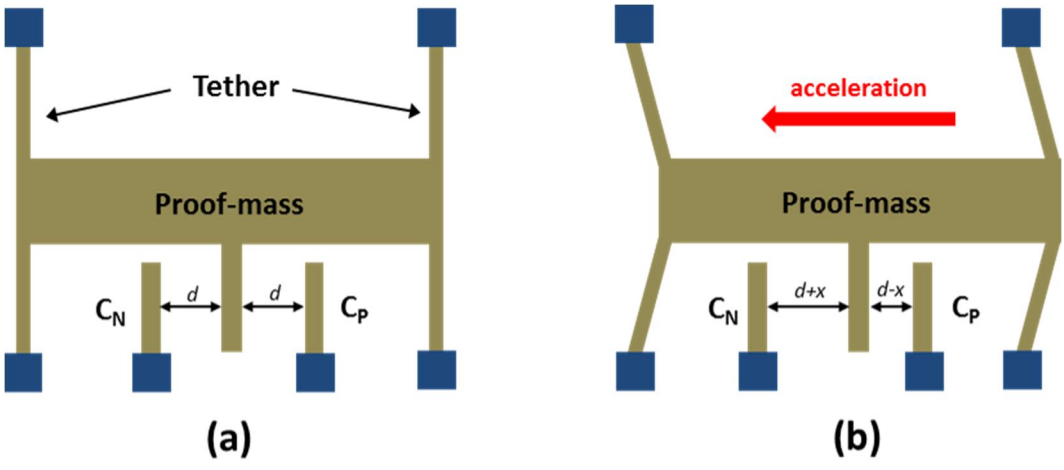


Figure 2. 2: Schematic diagram of capacitive accelerometer under (a) static and (b) accelerating condition

Figure 2. 2 shows the simplified diagram of capacitive accelerometer. During static condition (Figure 2. 2(a)), the distance between proof-mass and sensing electrodes is *d*, resulting sense capacitances C_P and C_N that are equivalent to equation (2-4), where ε_0 represents the permittivity, *A* as electrode area, and *d* as a capacitive gap, respectively.

$$C_P = C_N = \frac{\varepsilon_0 A}{d} \qquad (2\text{-}4)$$

The sensing electrodes are placed in a specific configuration so that the change of gap size due to device movement has opposite polarity between each other (Figure 2. 2(b)). The resulting differential capacitance is expressed as equation (2-5), where *x* is the displacement of proof-mass. The equation (2-5) can be further simplified as equation (2-6), assuming displacement *x* is far smaller than the gap size *d*.

$$\Delta C = C_P - C_N = \varepsilon_0 A\left(\frac{1}{d-x} - \frac{1}{d+x}\right) = \varepsilon_0 A\left(\frac{2x}{d^2 - x^2}\right) \qquad (2\text{-}5)$$

$$\Delta C \cong \frac{2\varepsilon_0 A}{d}\left(\frac{x}{d}\right) \quad (x \ll d) \qquad (2\text{-}6)$$

The scale factor, which is the amount of differential capacitance change with respect to the applied acceleration, is expressed as equation (2-7), where $\overrightarrow{a_{ext}}$ represents applied acceleration, and ω_0^2 as resonance frequency respectively.

$$\frac{\Delta C}{\overrightarrow{a_{ext}}} \cong \frac{2\varepsilon_0 A}{d^2}\left(\frac{M}{K}\right) = \frac{2\varepsilon_0 A}{d^2}\left(\frac{1}{\omega_0}\right)^2 \qquad (2\text{-}7)$$

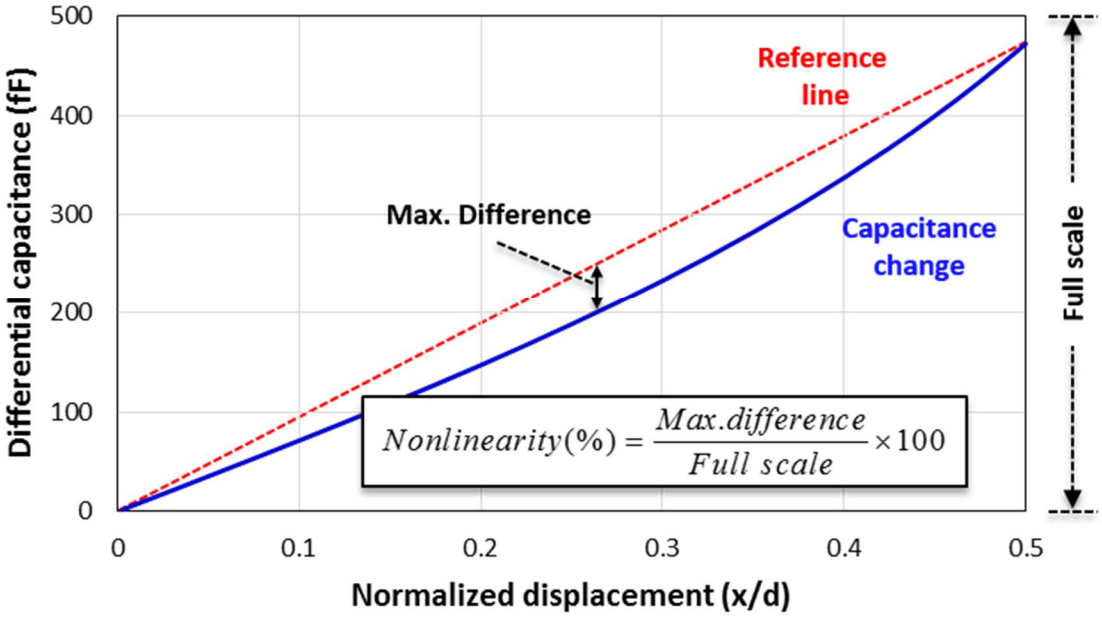


Figure 2. 3: Nonlinearity calculation on capacitive accelerometer

The fact that displacement x is located at the denominator of scale factor, implies that the relationship between capacitance change ΔC and applied acceleration $\vec{a}_{ext}$ would not be completely linear. Such nonlinearity can be measured by taking the maximum differences between actual capacitance change ΔC and theoretical line as shown on Figure 2. 3. As the displacement x during actual operation is far smaller than the gap size d, the capacitance change ΔC can be considered to have quasi-linear relationship with the applied acceleration $\vec{a}_{ext}$. However, when the device needs to sense high levels of accelerations (> 10 g), increased displacement on proof-mass would break such assumptions and worsen the nonlinearity performance. At such circumstances, resulting nonlinearity value may not meet the required specification for desired application. One possible solution to address such issue is to use closed-loop configuration, which employs electrostatic force to null out the excessive movement on the microstructure [30].

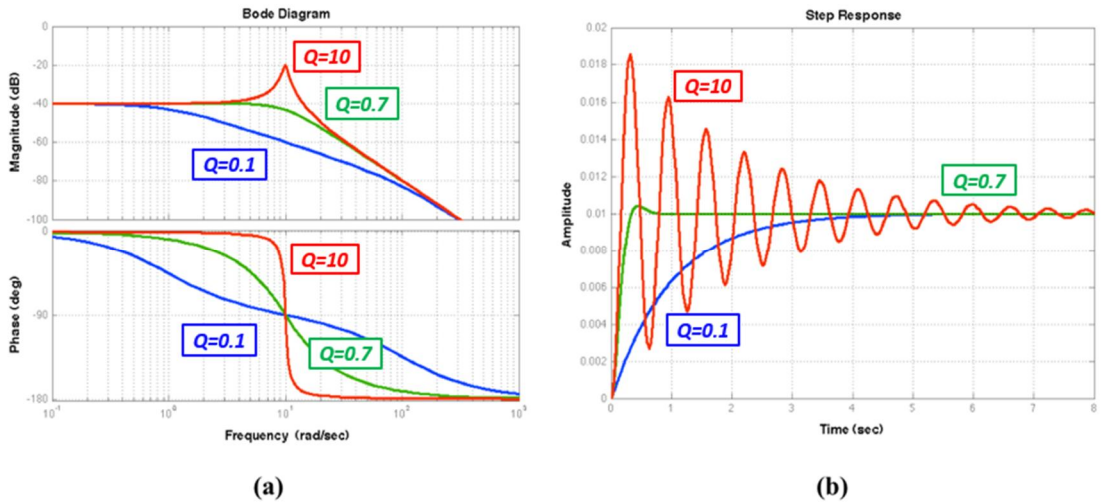


Figure 2. 4: (a) Frequency and (b) step response of accelerometer at different operating conditions

Depending on the quality factor *(Q)*, which is expressed as equation (2-8). the accelerometer operation can be divided into three categories; under-damped *(Q>0.707)*, critically-damped *(Q=0.707)*, and over-damped *(Q<0.707)*. Based on which condition does the accelerometer is operated, its dynamic behaviors can be different.

$$Q = \frac{\sqrt{KM}}{D} \quad (2\text{-}8)$$

The frequency and step response behaviors at different operating conditions are shown on Figure 2. 4. When the device operates at under-damped condition *(Q>0.707)*, the proof-mass experiences a resonant behavior, resulting in large overshoot and long settling time that deteriorate the overall system bandwidth and/or create a permanent damage to the microstructure [18],[31]. Due to such reasons, most of commercial MEMS accelerometer is designed to be operated at critically-damped *(Q=0.707)* or slightly over-damped *(Q<0.707)* conditions.

Still it should be noted that the damping should not be too large, as it deteriorates the operational bandwidth as shown in equation (2-9), where ζ denotes damping coefficient.

$$BW = \omega_0 \sqrt{1 - 2\zeta^2 + \sqrt{2 - 4\zeta^2 + 4\zeta^4}} \qquad (2\text{-}9)$$

The damping coefficient *(D)* of the capacitive accelerometer is mostly determined by the squeezed-film-damping *(D_{SFD})*, which is caused by the interaction between compressed air-molecules and microstructure. The analytical expression for squeezed-film-damping *(D_{SFD})* is shown on equation (2-10), where N_e stands for number of electrode, η_{eff} as viscosity of the ambient gas, l_e as electrode length, and h_e as electrode thickness, respectively.

$$D_{SFD} = N_e \eta_{eff} l_e \left(\frac{h_e}{d} \right)^3 \qquad (2\text{-}10)$$

The effective viscosity *(η_{eff})* can be expressed as equation (2-11) [32], where η is nominal viscosity coefficient (air: 18.5×10-6 Ns/m^2) and K_n as Knudsen number *(K_n)*, which indicates the ratio between the mean free path *(λ_0)* of the gaseous molecule and the representative physical length scale *(d)* of the microstructure [33].

$$\eta_{eff} = \frac{\eta}{1 + 9.638 K_n^{1.159}} \qquad (2\text{-}11)$$

At lower pressure level *(P_a),* where the amount of air molecules is scarce, the Knudsen number *(K_n)* is high and leads to reduction in effective viscosity *(η_{eff})* and thus squeezed-film-damping coefficient *(D_{SFD})*, which behavior is shown on Figure 2. 5.

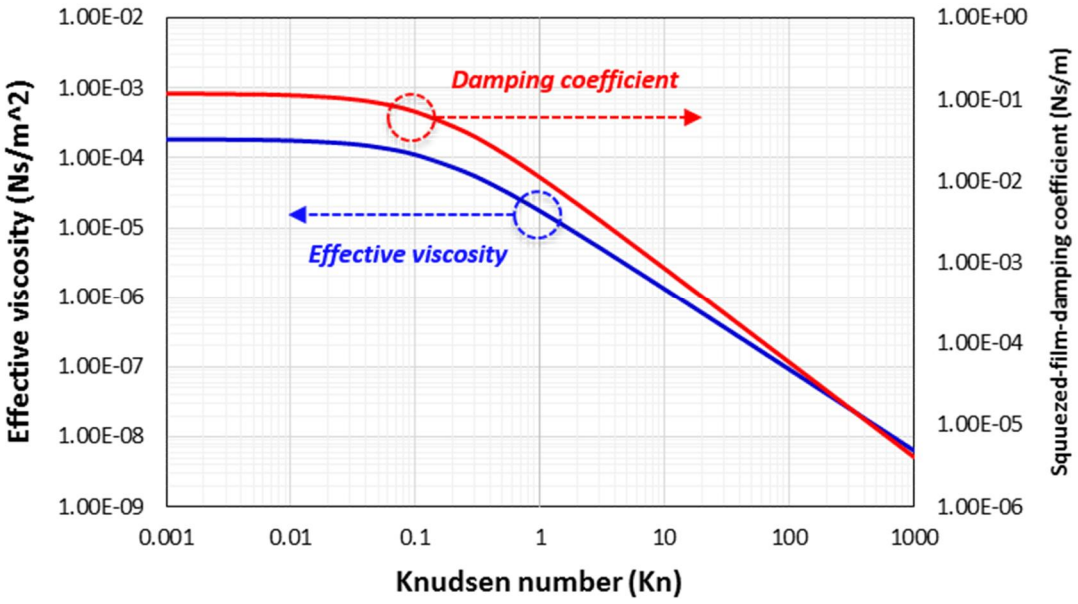


Figure 2. 5: Effective viscosity *(η_{eff})* and squeezed-film-damping coefficient *(D_{SFD})* with respect to different Knudsen number *(K_n)*

Consequently, when the pressure level gets low, the quality factor *(Q)* of the accelerometer is increased and pushes the operation toward the under-damped condition *($Q > 0.707$).*

The noise of the accelerometer *(TNEA)* is a combination between Brownian noise equivalent acceleration *(BNEA)* and circuit noise equivalent acceleration *(CNEA)* as shown in equation (2-12).

$$TNEA = \sqrt{BNEA^2 + CNEA^2} \qquad (2\text{-}12)$$

BNEA originates from the Brownian motion of air molecules inside the microstructure and expressed as equation (2-13), where k_B represents the Boltzmann constant, T as ambient temperature, and Q as quality factor of the device, respectively.

$$BNEA = \frac{\sqrt{4k_B TD}}{M} = \sqrt{\frac{4k_B T\omega_0}{MQ}} \qquad (2\text{-}13)$$

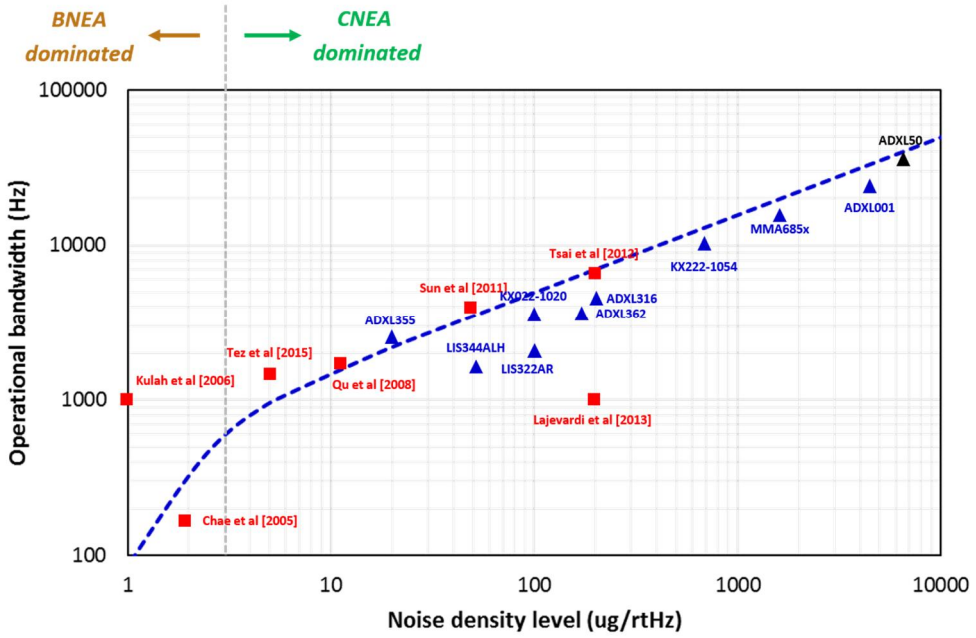


Figure 2. 6: Theoretical relationship between noise density level and resonant frequency of MEMS accelerometer

Circuit noise equivalent acceleration *(CNEA)* is caused by the noise of the interface circuit and expressed as equation (2-14). ΔC_{min} represents the capacitive resolution, which can be calculated by dividing the output voltage noise by the circuit gain (CV_{gain}).

$$CNEA = \frac{\Delta C_{\min}}{ScaleFactor} \approx \frac{\Delta C_{\min}}{2\varepsilon_0 A}\omega_0^2 d^2 = \frac{\Delta C_{\min}}{2\varepsilon_0 A}\frac{K}{M}d^2 \qquad (2\text{-}14)$$

The fact that both *BNEA* and *CNEA* has proportional relationship with device resonant frequency, makes it difficult for an accelerometer, which has wide operational bandwidth (i.e. high device resonant frequency) to achieve low-noise performance. A comprehensive theoretical analysis was conducted to validate this characteristic. Figure 2. 6 plots the resonant frequency with respect to *TNEA* level of MEMS accelerometer, which proof-mass *(M)* is 9.32e-9 kg, gap size (d) is 2 μm, sense capacitance is 500 fF, and ΔC_{min} is 1 aF/√Hz, respectively. The relationship between the noise and the resonant frequency gets different depending on whether the *TNEA* is dominated by *BNEA* or *CNEA*. Still in

either cases, it is observed that both parameters form an inversely proportional relationship each other. It is interesting to see the performances of existing commercial accelerometers and the accelerometers reported from academia falls with the same trend with theoretical relationship between resonant frequency and noise density level.

The output of inertial sensor undergoes a drift over time, which eventually accumulates as time-integrated error that deteriorates the overall accuracy when used as a navigational platform. Such performances can be measured using Allan Deviation (ADEV) analysis [34] by measuring the output of accelerometer under static position for a long period, and integrating each data point with different number of samples (τ) (*i.e.* time-period). Figure 2. 7 shows an example of ADEV plot, where each value is plotted with respect to different integration period (τ). The point where the slope is zero is called as bias instability, which is caused by the white noise. The point where slope is -1/2 is called the Velocity Random Walk (VRW), and this is caused by the flicker noise of the electronics that is interfaced with the MEMS device.

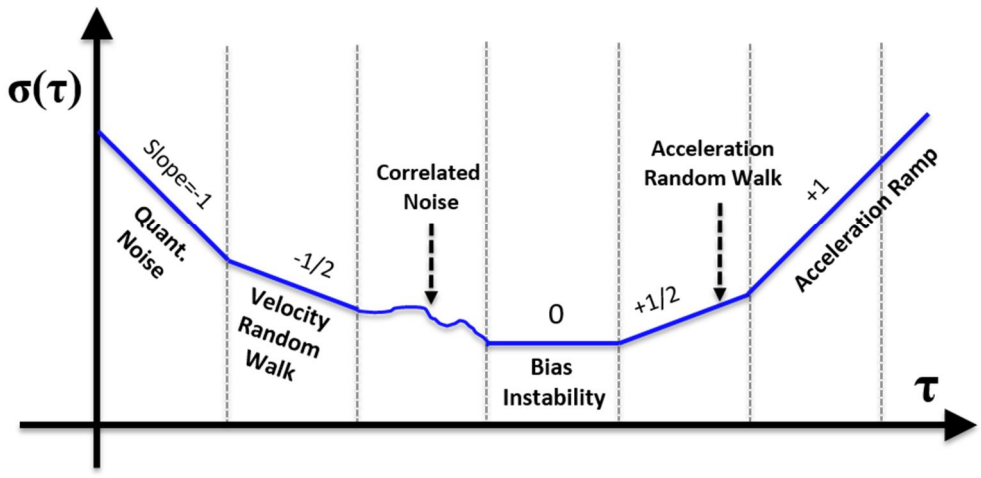


Figure 2. 7: Example of Allan deviation plot annotating system performance parameters

2.2. DESIGN METHODOLOGY

The fact that both resonant frequency and noise level have directly counteracting relationship each other (Figure 2. 6), makes it extremely hard to design an accelerometer that provides both operational bandwidth and precision resolution level. However, it should be noted that both *BNEA* and *CNEA* shown in equation (2-13) and (2-14) are also function of other design parameters. For example, *CNEA* has a strong relationship with electrode geometry, meaning that by utilizing high aspect ratio sensing gap that is scaled down to sub-micron range, the accelerometer can compensate the increase in the noise due to high resonant frequency. Furthermore, as *BNEA* is inversely proportional to the quality factor *Q*, operating accelerometer in low-pressure level would guarantee improved noise performance.

This relationship is shown on Figure 2. 8, where the total noise of accelerometer *(TNEA)* decreases significantly by scaling down gap size and ambient pressure level. When the gap size is reduced from 2 μm to 500 nm at 760 Torr pressure level, *TNEA* improves by 10 times. Additionally, by lowering the pressure level down to 10 Torr, *TNEA* improves even more thanks to reduced *BNEA*, making the optimum gap size near 300 nm. Such improvement can be utilized to implement accelerometer with low noise and wide operational bandwidth. It should be noted that although presented accelerometer is operated at low-pressure environment, the quality factor is still near 0.5 at 10 Torr level, meaning its operation would be critically damped condition. Such operation was not possible in conventional accelerometer, which has orders of magnitude large sensing gap compared to presented design, as doing so would result in instability behaviors, such as large overshoot or long settling time [18],[31].

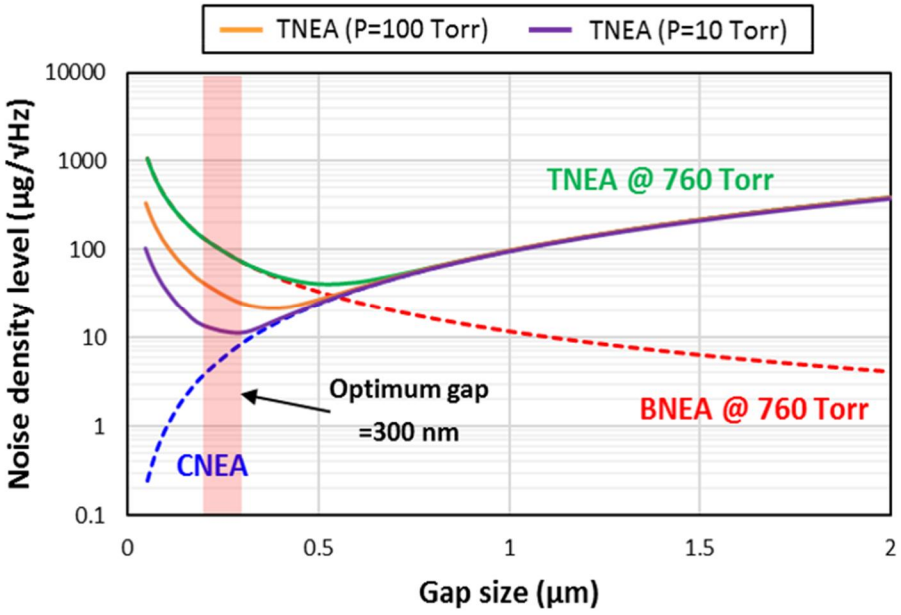


Figure 2. 8: Accelerometer noise with respect to gap size at different pressure level

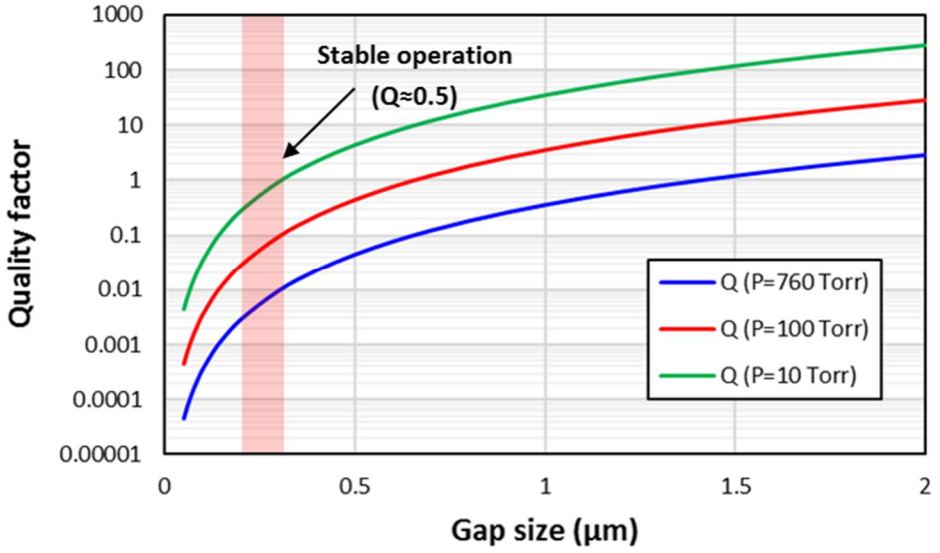


Figure 2. 9: Quality factor of accelerometer with respect to gap size at different pressure level

This behavior was enabled by increased squeezed-film-damping (D_{SFD}), which is shown in equation (2-10). As the damping has strong relationship with the electrode geometry, utilizing gap size (< 300 nm) that is orders of magnitude narrower than that of conventional accelerometer (1~3 µm) boosts the damping to the point where the quasi-static accelerometer reaches a stable operating point at low-pressure level.

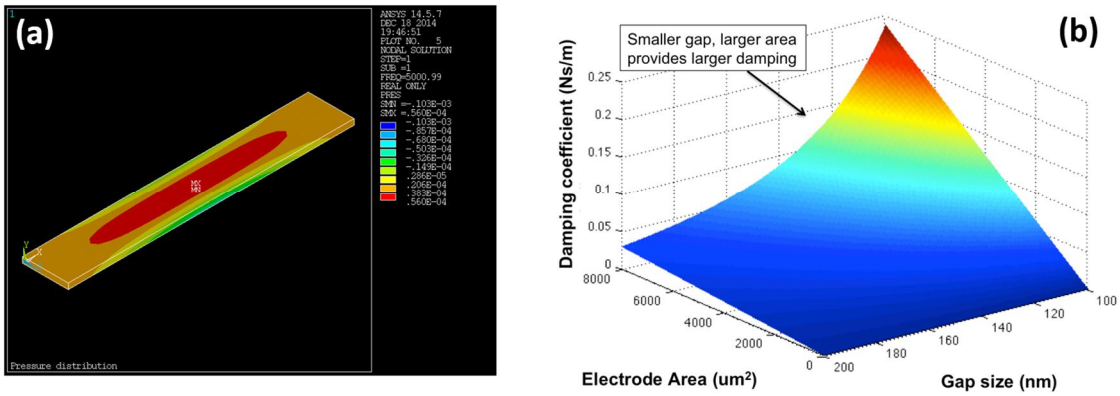


Figure 2. 10: Squeezed-film-damping simulation of clamped-clamped beam structure using ANSYS™

Finite-Element-Method (FEM) analysis using ANSYS simulator was used to validate the effectiveness of using nano-gap electrode to attain stability in low-pressure operation. Damping coefficient of clamped-clamped beam with different gap sizes and surface area was extracted under 10 Torr pressure level. Simulation result on Figure 2. 10 shows the significant increase in damping coefficient by having a narrow and wide electrode, pushing the operation over-damped *(Q<0.707)* from under-damped *(Q>0.707)* condition. The possibility of operating quasi-static accelerometer in low-pressure level without stability issues opens a new possibility of implementing single-chip multi-sensor platform. Compared to other methods, such as resonant accelerometer [16]-[17], closed-loop interface topology [18], or separate wafer-level cavity with different pressure (Figure 1. 6) that are used to operate accelerometer in vacuums, proposed methodology provides a simple, but cost-effective alternative.

2.3. *GEN-1* ACCELEROMETER DESIGN

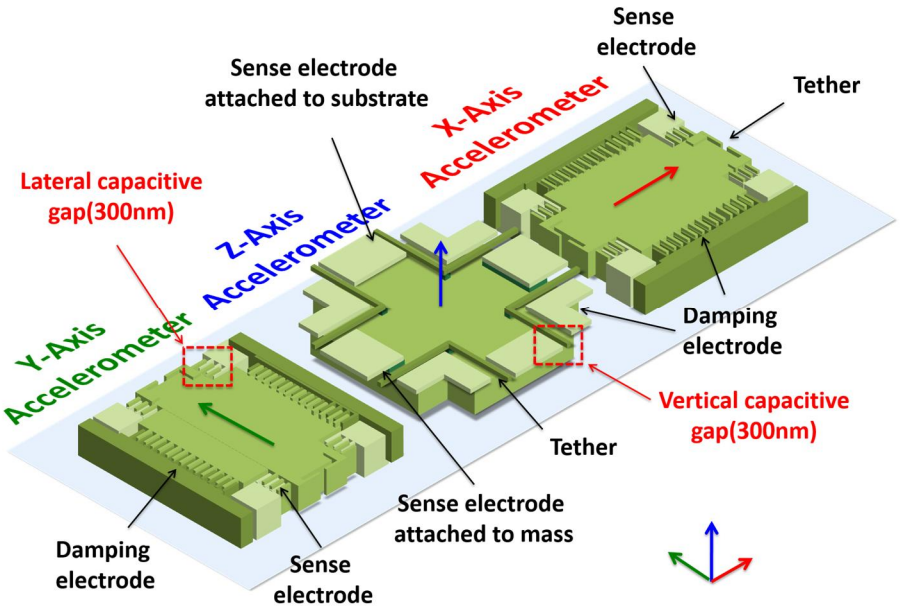


Figure 2. 11: Schematic diagram of proposed tri-axial accelerometer design

Figure 2. 11 shows the schematic diagram of proposed accelerometer [38], which is comprised of three separate single-axis devices. Presented designs are operated under wafer-level-packaged environment (1~10 Torr) with different resonant devices such as gyroscopes and timing element [39]-[40]. To ensure our accelerometer has wide operational bandwidth (> 10kHz), the lower bound of the device resonant frequency was set to 10 kHz. To determine the required gap size of the accelerometer, thorough design optimization analysis was conducted while ΔC_{min} was assumed as 1 aF/√Hz, pressure level of 10 Torr and the sensor size as 1 mm × 1 mm × 40 μm. Figure 2. 12 shows the accelerometer noise with respect to the gap size at different resonant frequencies. Whereas the *CNEA* increases with larger gap size due to less capacitive sensitivity, the *BNEA* decreases as the damping coefficient gets reduced. Such behaviors between each noise results in optimum gap size near 300 nm.

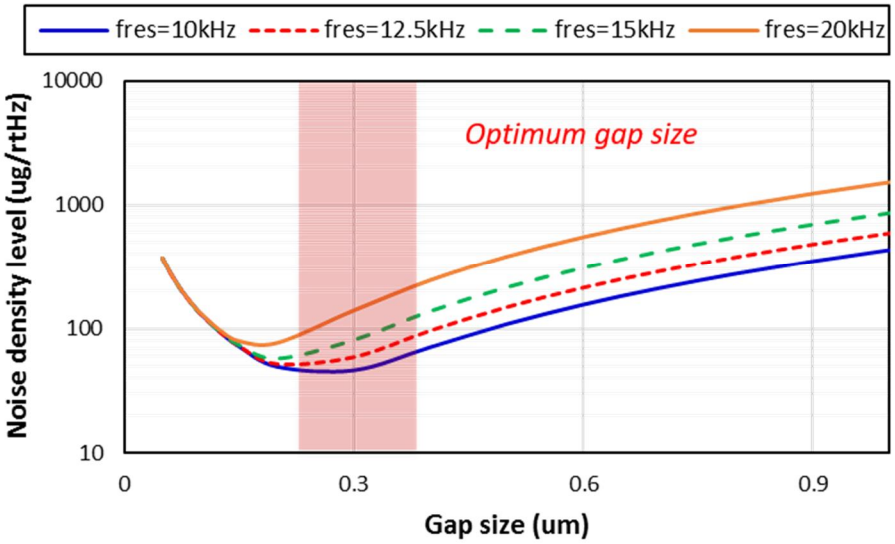


Figure 2. 12: Accelerometer noise with respect to gap size at different resonant frequency

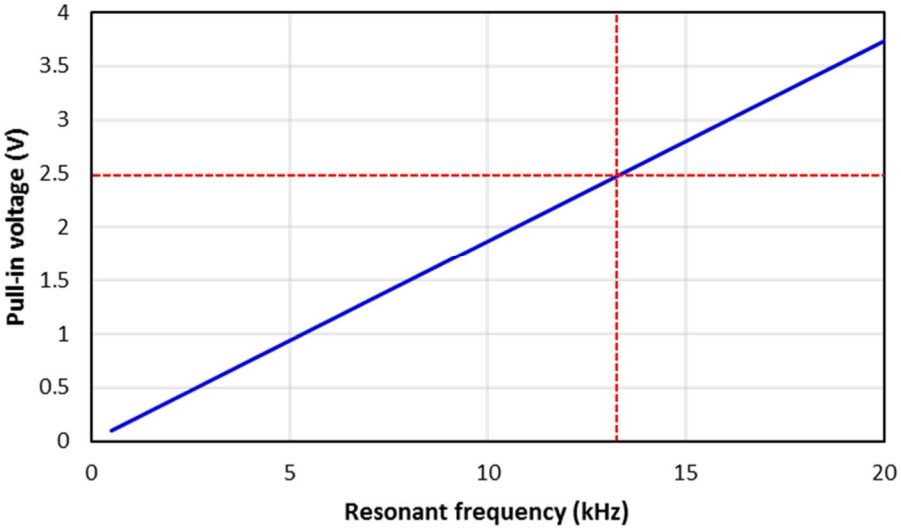


Figure 2. 13: Pull-in voltage of accelerometer across different resonant frequency

On the other hand, the resonance frequency cannot be made too low as it would lower the pull-in voltage limit, the maximum allowable electrical potential between microstructures as shown in equation (2-15) [41].

$$V_{Pullin} = \sqrt{\frac{8}{27}\frac{Kd^3}{\varepsilon_0 A}} = \sqrt{\frac{8}{27}\frac{Md^3}{\varepsilon_0 A}}\omega_0 \qquad (2\text{-}15)$$

As the MEMS accelerometer is interfaced with readout electronics, the pull-in voltage is defined based on the supply voltage of the circuit, which is 2.5 V. Figure 2. 13 shows that the lower bound of resonant frequency is set as 13.5 kHz.

The proposed accelerometer is wafer-level-packaged in low-pressure environment, which is between 1 to 10 Torr. To ensure stable response under such circumstances, the quality factor *(Q)* of the accelerometer needs to be near critically-damped region *(Q=0.707)*. Figure 2. 14 shows the calculated quality factor *(Q)* of the proposed accelerometer with respect to different pressure level, based on predetermined gap size (≈300 nm) and the resonance frequency (>13.5 kHz). At the pressure level between 1 to 10 Torr, the lowest quality factor of the sensor is 35.47, which is too high to guarantee its stable operation. The number of sensing electrodes can be increased to reach the stable point, but at the expense of sacrificing the pull-in voltage. To address the such difficulty, a novel damping electrode structure, which simplified schematic diagram is shown on Figure 2. 15 is incorporated into the design. The proposed structure has an equal gap size as the sensing electrode but electronically tied to the substrate, creating a zero potential between microstructures. As there is no induced electrostatic force, the number of damping electrodes only affects the squeezed-film-damping coefficient, but not on the pull-in voltage. Figure 2. 14 shows that once the damping electrode is used, the quality factor *(Q)* gets reduced significantly so that the device reaches the stable point at the pressure level between 1 to 10 Torr. During analysis, the accelerometer was assumed to have 200 damping fingers with 100 μm length and 40 μm height.

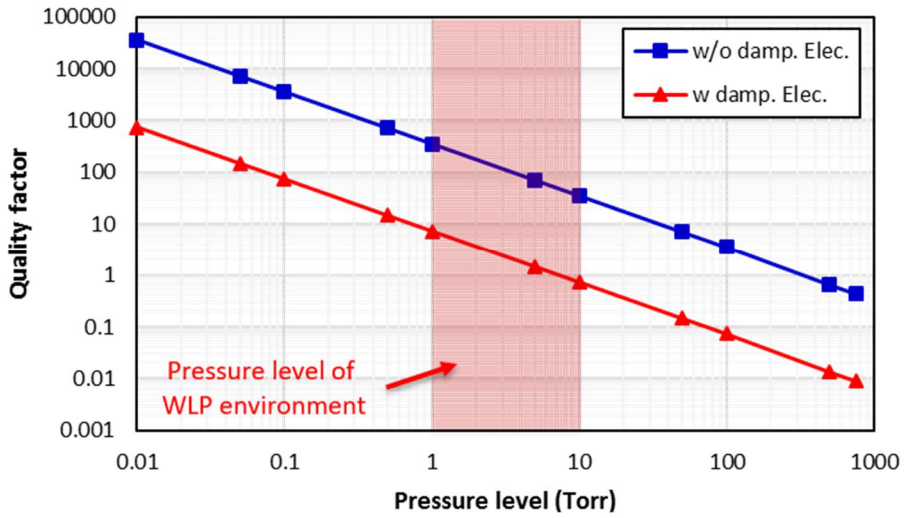


Figure 2. 14: Quality factor and pull-in voltage of accelerometer with respect to number of electrodes under different configuration (damping electrode)

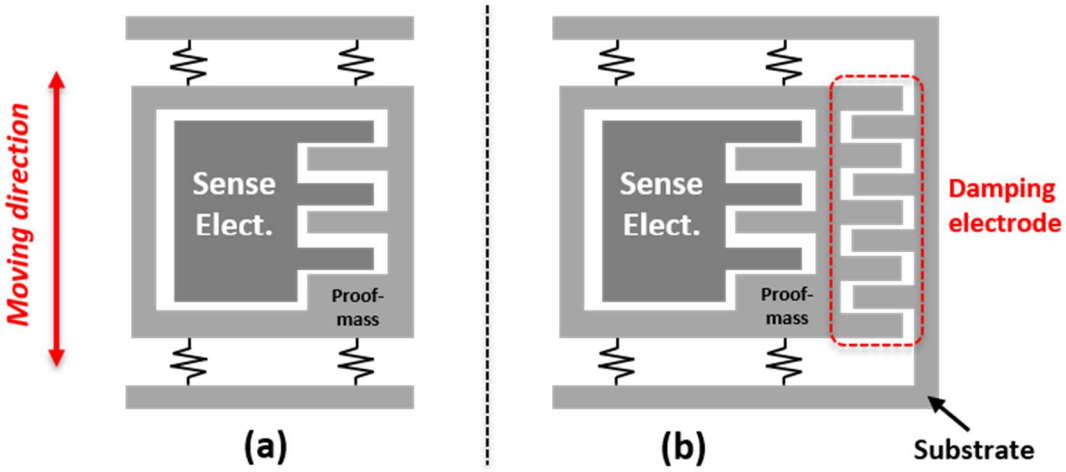


Figure 2. 15: Simplified schematic diagram of the accelerometer (a) with and (b) without damping electrode configuration

Derived device parameters (resonant frequency, sensing capacitance, number of damping electrodes, etc) from the design analysis were used to implement both *Gen-1* in-plane and out-of-plane accelerometers, which schematic diagram is shown on Figure 2. 16(a) and (b). Both design employs a differential sensing topology to cancel out the common-mode noise such as substrate coupling or large static capacitance. The in-plane accelerometer has four sense electrodes placed at each corner of the proof-mass. The out-

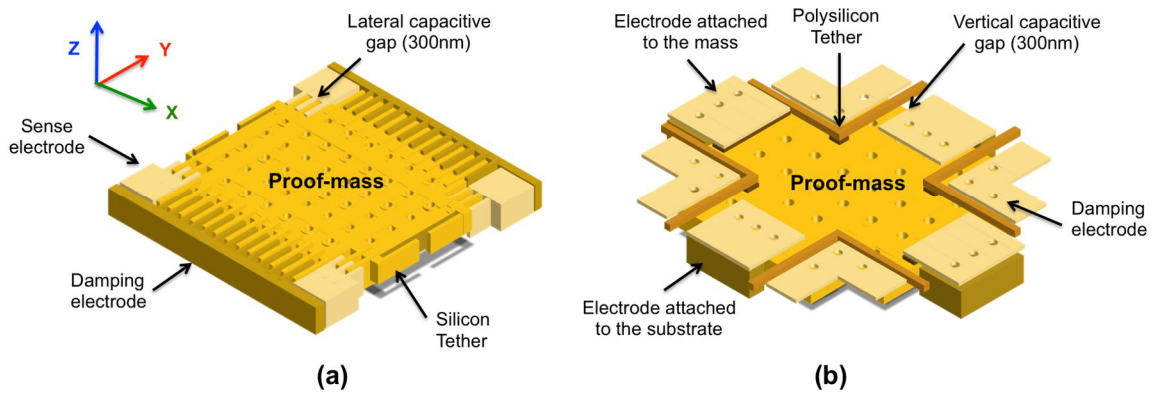


Figure 2. 16: Schematic diagram of (a) in-plane and (b) out-of-plane *Gen-1* accelerometer

of-plane accelerometer has two sense electrodes attached to the substrate whereas the other two electrodes are connected to the proof-mass, generating an out-of-plane differential capacitance change when the external force is exerted [38],[42],[43]. The damping electrodes are carefully placed perpendicular to the axis of displacement to maximize the amount of squeezed-film damping *(D_{SFD})*, while its area is tailored to meet the stability requirement. Both designs employ 300 nm sensing gap in both lateral and vertical directions.

2.3.1. Simulation Analysis

Proposed accelerometers designs are extensively simulated using ANSYS FEM tools to extract various system parameters such as resonant frequency, scale factor, and damping coefficient. Figure 2. 17 and Figure 2. 18 show the modal analysis of the in-plane and out-of-plane accelerometer. The parasitic resonant modes ($2^{nd}/3^{rd}/4^{th}$) were intentionally designed to be far apart from the dominant frequency to suppress any unwanted coupling. The simulated resonant frequencies are 13.647 kHz and 16.76 kHz. The extracted stiffness was 468 N/m and 610.7 N/m for each design.

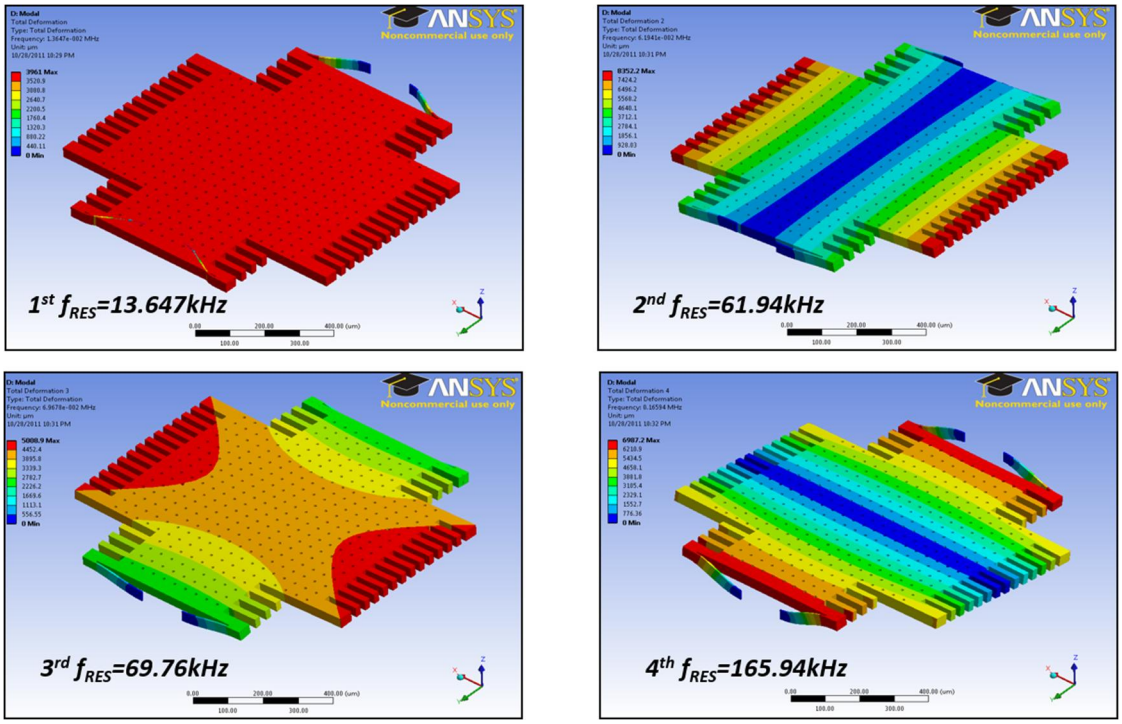


Figure 2. 17: Modal simulation result of in-plane accelerometer

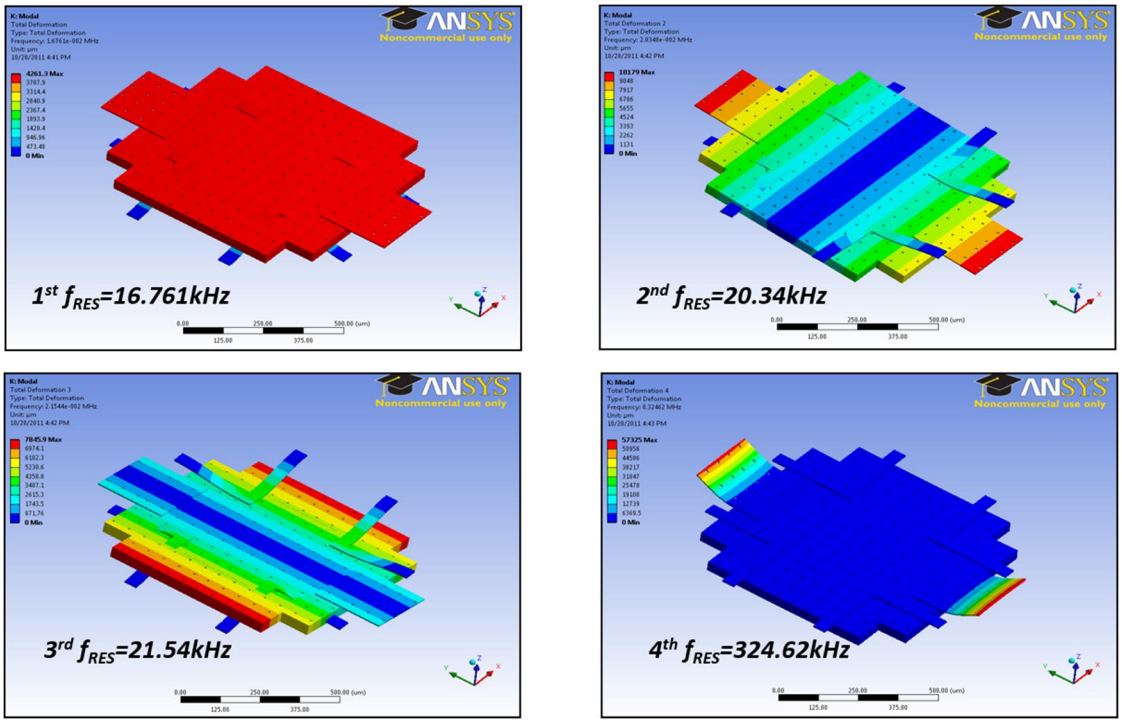


Figure 2. 18: Modal simulation result of out-of-plane accelerometer

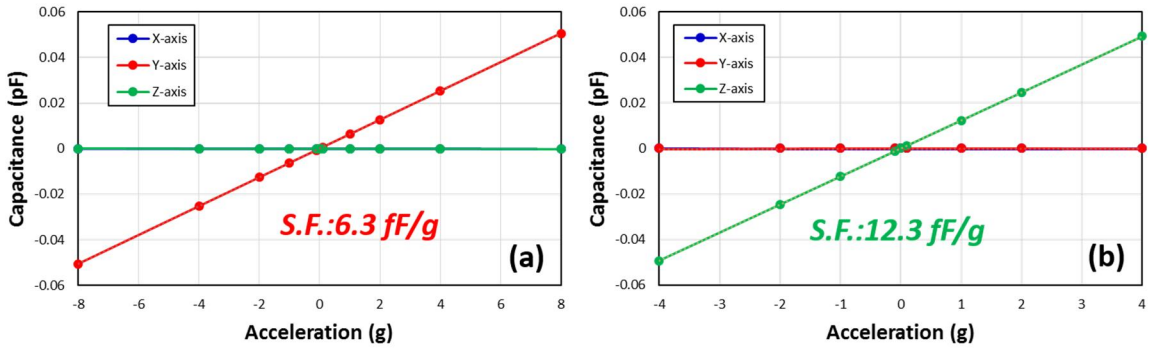


Figure 2. 19: Simulated scale factor of (a) in-plane and (b) out-of-plane accelerometer

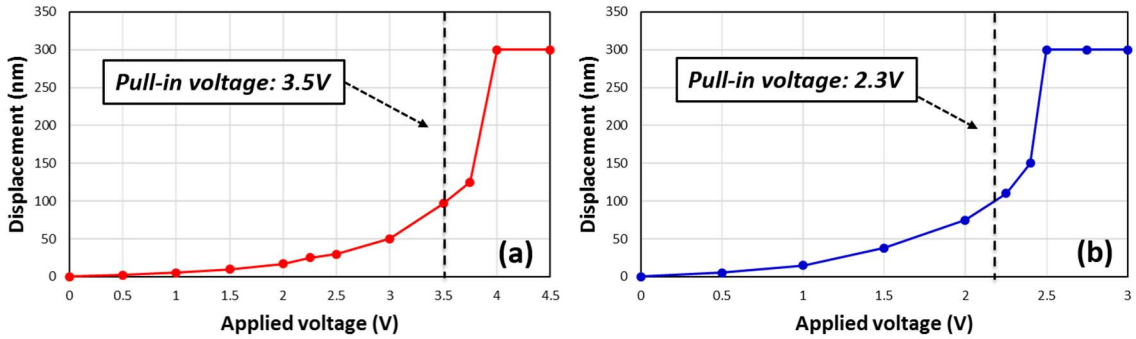


Figure 2. 20: Pull-in simulation result of *Gen-1* (a) in-plane and (b) out-of-plane accelerometer

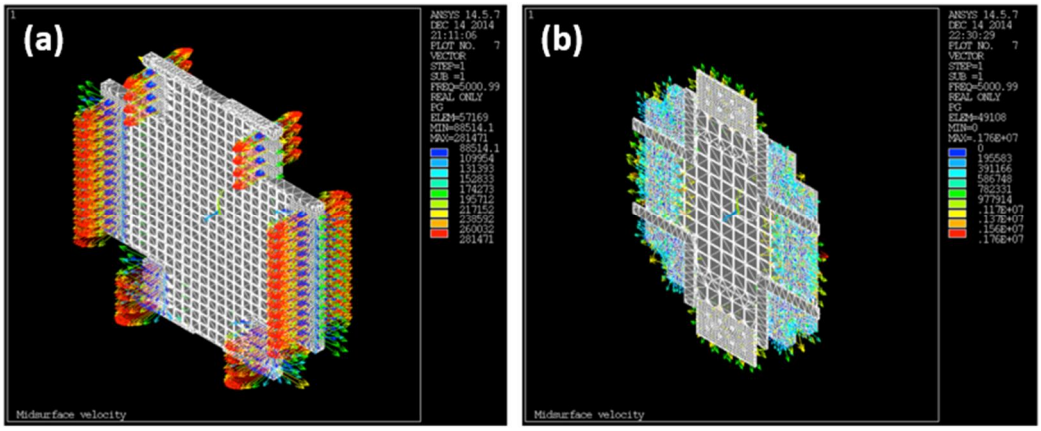


Figure 2. 21: Squeezed film damping simulation of (a) in-plane and (b) out-of-plane accelerometer

The capacitive sensitivity and the pull-in voltage level were simulated using electrostatic TRANS126 element. Figure 2. 19 and Figure 2. 20 show the scale factor of 6.3 fF/g and 12.3 fF/g, and the pull-in voltage of 3.5 V and 2.3 V for both in-plane and out-of-plane designs respectively. The stability of the proposed accelerometer is also evaluated

by running a squeezed-film-damping *(D_{SFD})* simulation using FLUID136 element (Figure 2. 21). Simulated quality factor is 0.54 and 0.923 for in-plane and out-of-plane accelerometer at 10 Torr pressure level, which satisfies the stability requirement.

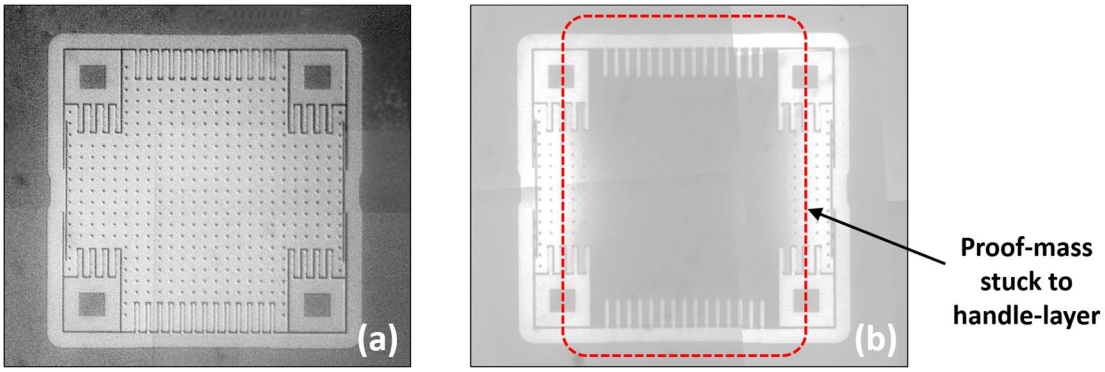


Figure 2. 22: IR microphotograph comparison between accelerometer that (a) was properly released and (b) suffered from stiction

During fabrication process, the proof-mass may adhere to sense electrodes or substrate and results in stiction [44], which can be a catastrophic as it directly affects the device operation and the overall fabrication yield. Figure 2. 22 shows the Infra-red (IR) microphotograph of the in-plane accelerometers that is (a) properly released (i.e. functional) and (b) suffers from stiction. The light grey color at the Figure 2. 22(a) indicates the region that has been released successfully. However, when the device experiences the stiction, it would have dark grey color at the proof-mass as shown in Figure 2. 22(b). This indicates that entire proof-mass has been stuck to handle layer of the silicon substrate.

The stiction is mostly caused by the capillary force of the thin liquid layer (i.e. wet etchant), which is located at the narrow capacitive gap or box-oxide layer during releasing process as shown on Figure 2. 23 [44]. The capillary force can be expressed as equation (2-16), where A is wetted area, γ_{la} is the surface tension of the liquid-air surface, θ_c is the contact angle between liquid and solid in air, and g is the liquid layer thickness respectively.

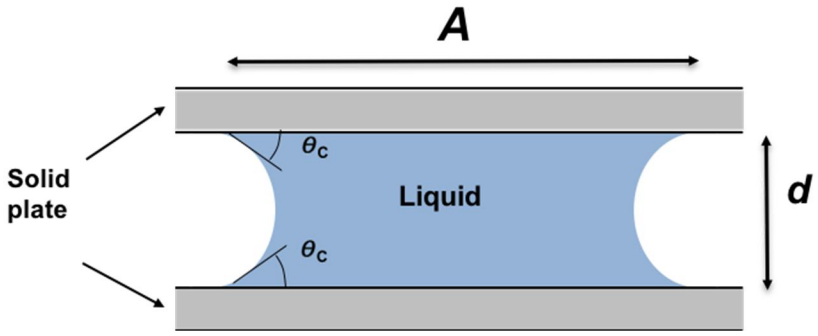


Figure 2. 23: Schematic illustration of liquid layer between two mechanical plates; Pressure difference at liquid-air interface creates adhesive force (Capillary force)

As we are utilizing capacitive gap (300 nm) that is much smaller than that of the conventional design (1 ~ 3 μm), the proposed accelerometer can be very susceptible to stiction.

$$F = \frac{2A\gamma_{la}\cos\theta_c}{g} \qquad (2\text{-}16)$$

Although it is difficult to estimate the exact capillary force during release process, we can still evaluate the possibility of stiction by comparing the restoring forces with existing design that was successfully released without any stiction. The restoring force [45], which is the multiplication between the stiffness *(K)* and the minimum gap size *(d)*, indicates the amount of force that tries to restore the movable proof-mass into original position under maximum displacement (i.e. gap size). Table 2. 1 shows the comparison of restoring force between the proposed accelerometer design and other works that had been successfully fabricated earlier. As the sensing fingers can be another possible cause for the stiction due to low stiffness *(K)* coming from its long and narrow shape, the beam stiffness was also calculated and compared with that of prior designs in Table 2. 2. As all the

calculated restoring forces and stiffness are similar or larger than prior works, it is concluded that proposed accelerometers are unlikely to experience stiction.

Table 2. 1: Restoring force comparison between different designs

Design	Stiffness	Gap size	Restoring force
P. Monajemi et al [46]	10.3 N/m	1.3 μm	13.39 μN
R. Abdolvand et al [12]	52.5 N/m	4 μm	210 μN
Proposed in-plane design [38]	468 N/m	300 nm	140.4 μN
Proposed out-of-plane design [38]	610.7 N/m	300 nm	183.21 μN

Table 2. 2: Stiffness comparison for sensing electrode

Design	Width	Length	Height	Beam stiffness
P. Monajemi et al [46]	6 μm	820 μm	60 μm	3.97 N/m
R. Abdolvand et al [12]	10 μm	700 μm	100 μm	49.27 N/m
In-plane design [38]	20 μm	100 μm	40 μm	54080 N/m
Out-of-plane design [38]	250 μm	100 nm	6.5 μm	3437.9 N/m

2.3.2. FABRICATION AND MEASUREMENT RESULT

Both in-plane and out-of-plane accelerometers were fabricated on a 40 μm thick silicon-on-insulator (SOI) wafer using high-aspect ratio combined poly and single crystalline-silicon (HARPSS) process [39]-[40] as shown on Figure 2. 24. The entire fabrication starts with (a) the etching of 5 μm width DRIE trenches on a silicon wafer, which defines the geometries of the mechanical structure. (b) Then the sacrificial oxide layer of 300 nm is thermally grown to define lateral capacitive gaps, and (c) the remaining trench is filled with poly-silicon using LPCVD. If the trench does not have the HARPSS gap, it will be (b) filled with TEOS (Tetraethyl orthosilicate) oxide instead. Once the process is done, the 2nd oxide is deposited and further patterned to define top and bridging electrode, and 300 nm sacrificial layer is grown additionally to locate the out-of-plane

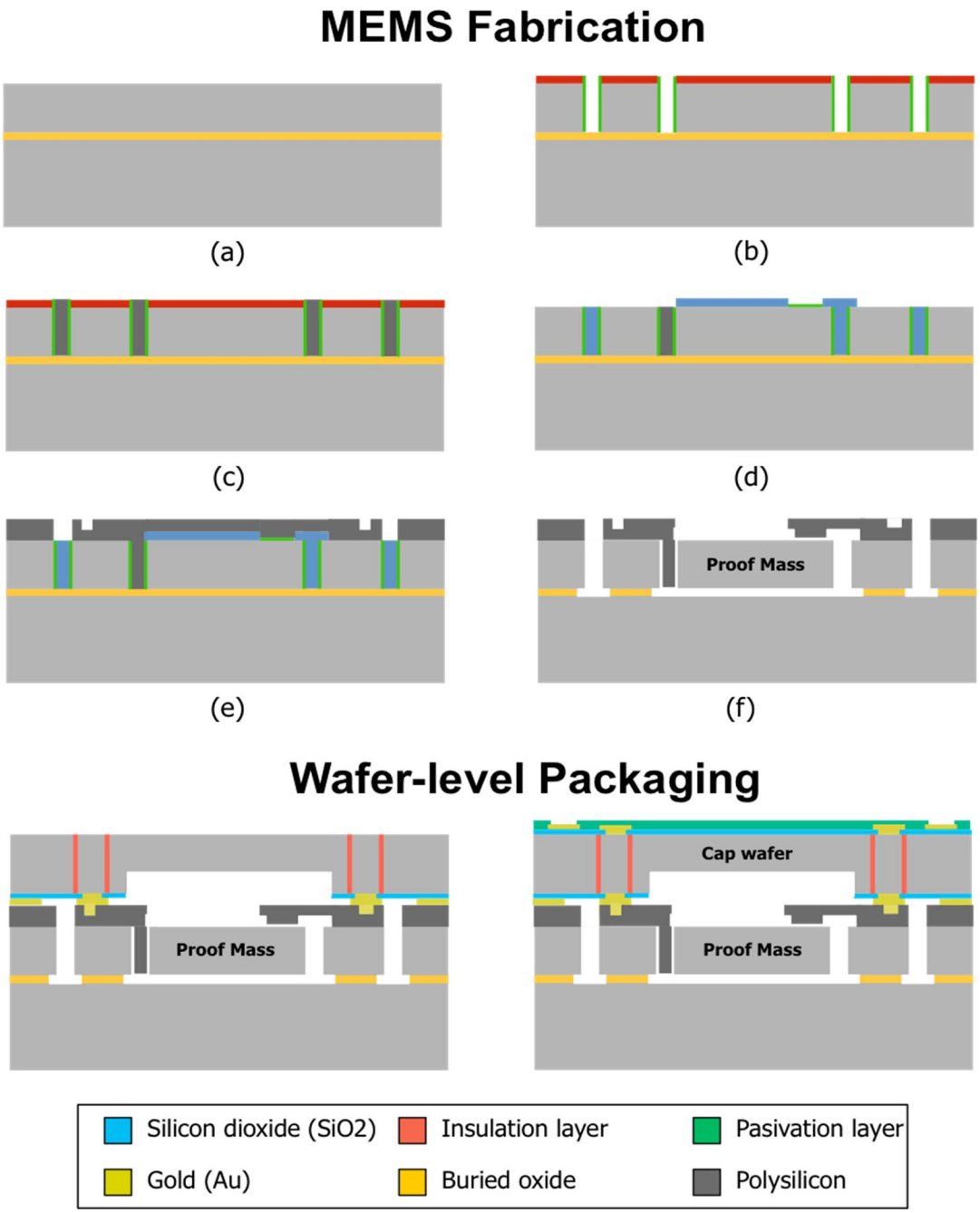


Figure 2. 24: Fabrication process diagram of MEMS accelerometer and its wafer-level packaging

sensing gaps, followed by (e) the deposition of poly-silicon layer. This layer is patterned to define top-electrodes and flexure tether for the out-of-plane direction. Finally, (f) entire devices are released in hydrofluoric acid (HF).

MEMS sensor is subsequently bonded to the capping wafer to provide a hermetic wafer-level vacuum-packaging (1~10 Torr). The capping wafer is processed separately by defining trenches and filling it with an insulator to implement through-silicon-via (TSV). As the wafer has low resistivity, the TSV provides a low-resistive path between the exterior pads and the inner MEMS device. A recess cavity was etched before the capping process and the gold patterns were defined to allow eutectic bonding with the MEMS wafer. After the sealing, gold metal traces and pads are deposited on top of the capping wafer.

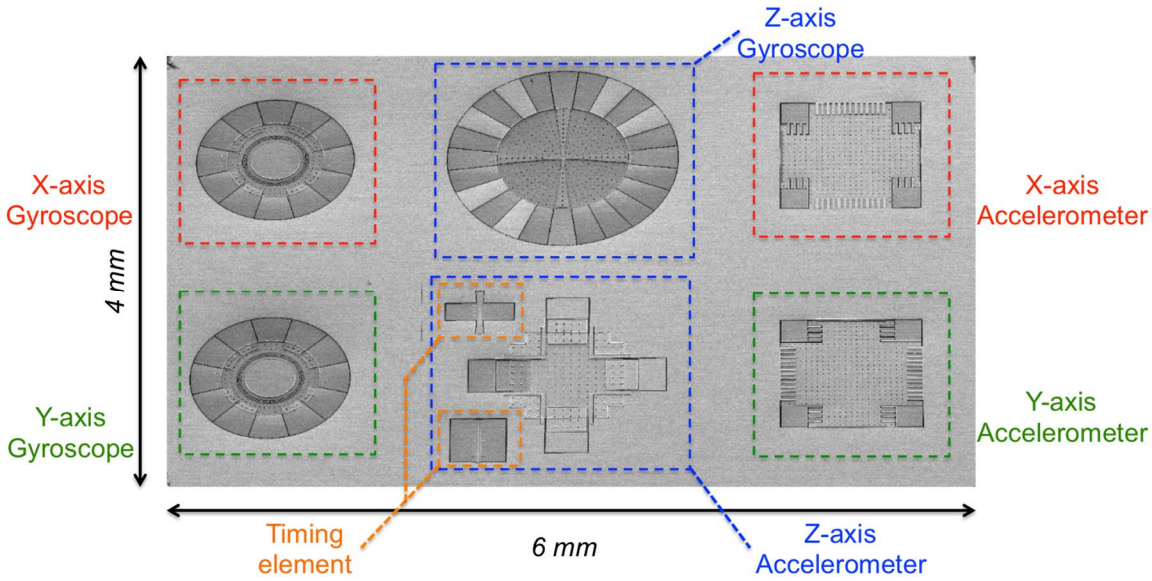


Figure 2. 25: SEM view of fabricated *Gen-1* accelerometer along with three-axis gyroscope and timing resonators

Proposed accelerometers were fabricated conjunction with three-axis vibratory gyroscopes [40][47] and timing resonator [48] on a common silicon substrate to enable single-chip timing and inertial measurement unit (Figure 2. 25). Figure 2. 26(a) and (b) shows the SEM photographs of the stand-alone in-plane and out-of-plane accelerometer, where 300 nm vertical and lateral gaps are also visible on Figure 2. 26(c) and (d). Figure 2. 27 shows the SEM view of wafer-level-packaged in-plane accelerometer, where the half portion of its capping wafer is intentionally pulled off to expose the inner MEMS.

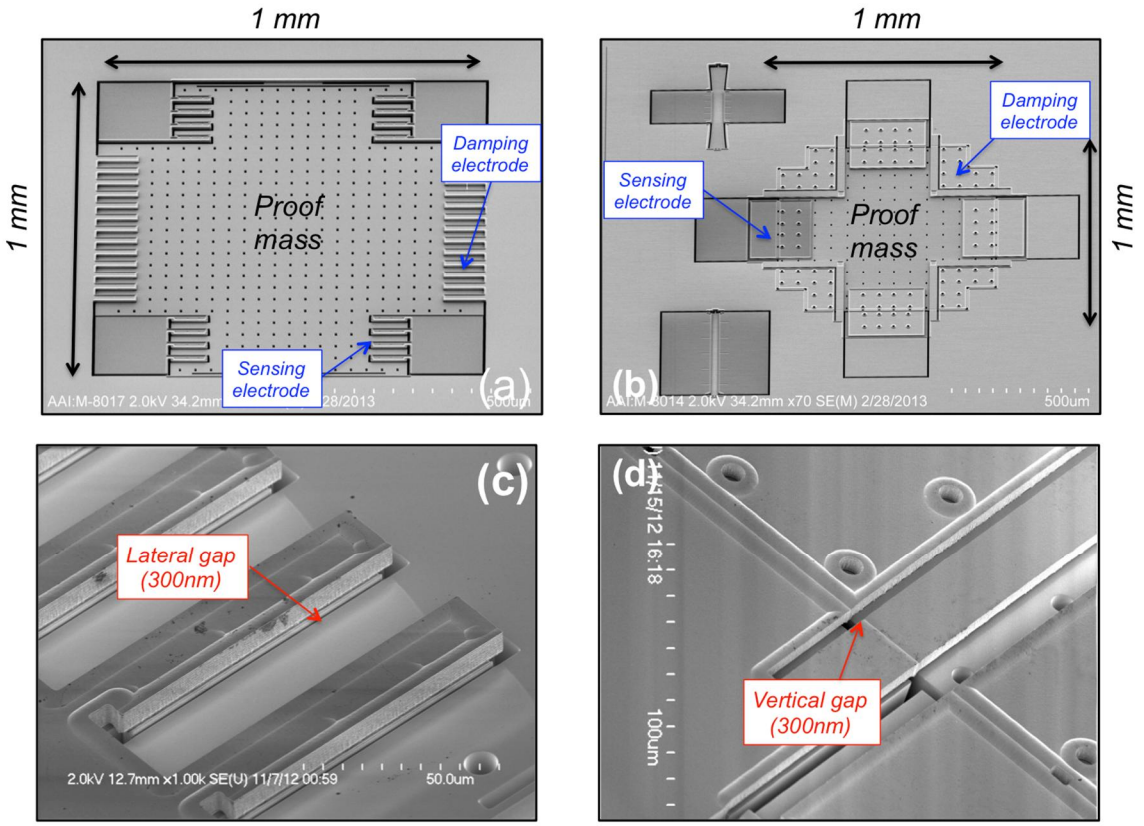


Figure 2. 26: SEM view of *Gen-1* (a) in-plane and (b) out-of-plane accelerometer, Closed-up view in (c) lateral capacitive gap and (d) vertical capacitive gap

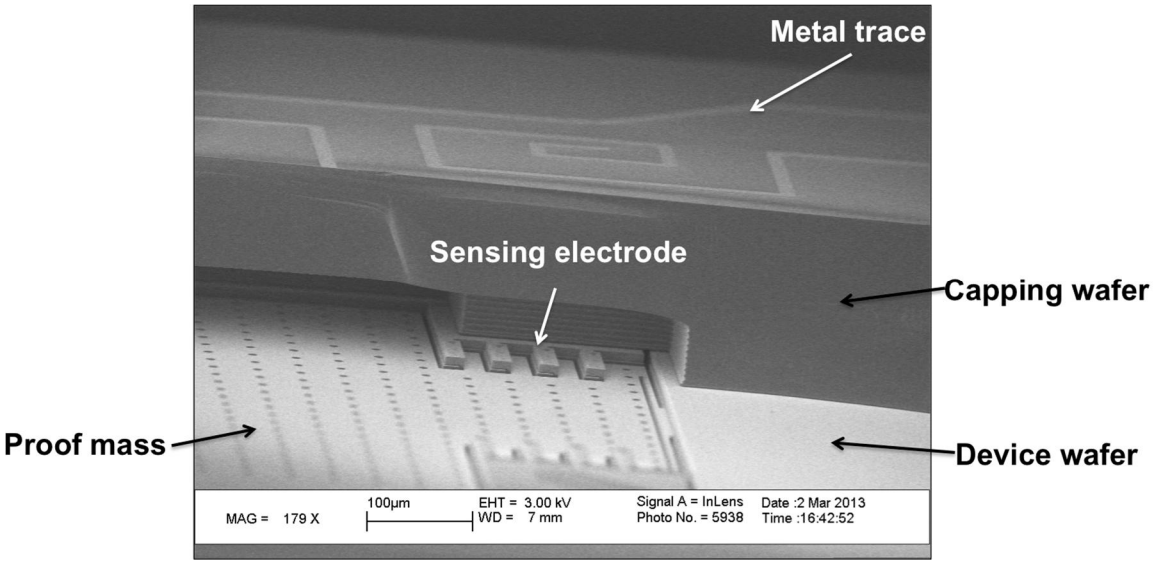


Figure 2. 27: SEM photo of wafer-level packaged (WLP) *Gen-1* in-plane accelerometer; Part of the capped wafer was intentionally pulled off to show the inner MEMS

The functionality of the fabricated MEMS accelerometers was first verified by measuring resonance response by placing an uncapped wafer inside the vacuum probe station as shown on Figure 2. 28. Two sense electrodes were connected to the actuation port, and the other electrodes are tied to the readout-channel of network analyzer (Figure 2. 28(b)). The pressure level was pulled down to 50 mTorr to minimize the amount of air damping, and observe the resonance response. Polarization voltage (V_P) of 0.5 V is applied to bias the proof-mass and to induce sufficient electrostatic force for the actuation. The frequency responses are shown on Figure 2. 29(a) and (b), where each resonance peak was observed at 16.2 kHz and 14.5 kHz for in-plane and out-of-plane accelerometers respectively. This is in good agreement with the simulation result shown in Figure 2. 17 and Figure 2. 18. Frequency discrepancy of 1~2 kHz seems to be caused by the process variation on mechanical spring during fabrication. When the pressure level increases to 1 Torr, the resonance peak diminishes, which confirms the stability of accelerometer under wafer-level-packaged low-pressure environment (1~10 Torr).

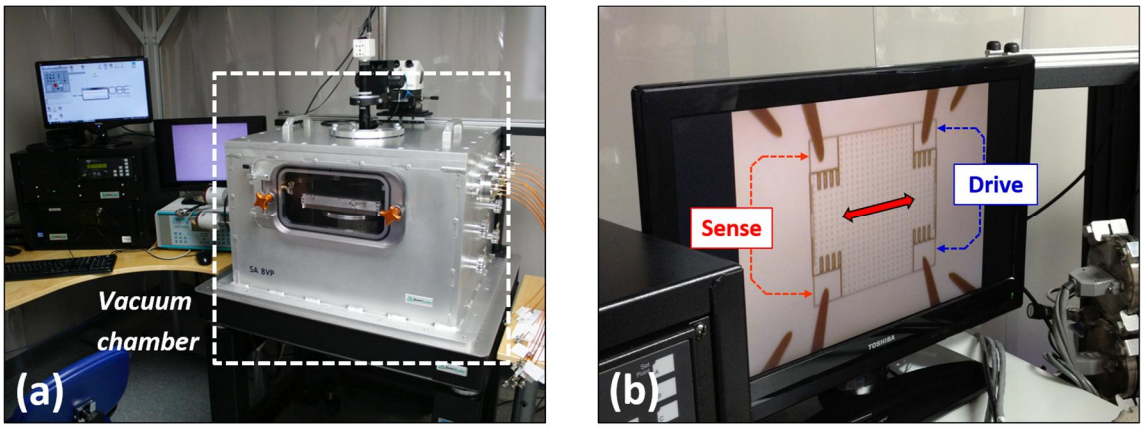


Figure 2. 28: Photo of (a) vacuum prober measurement setup and (b) probe-card connection to the in-plane accelerometer

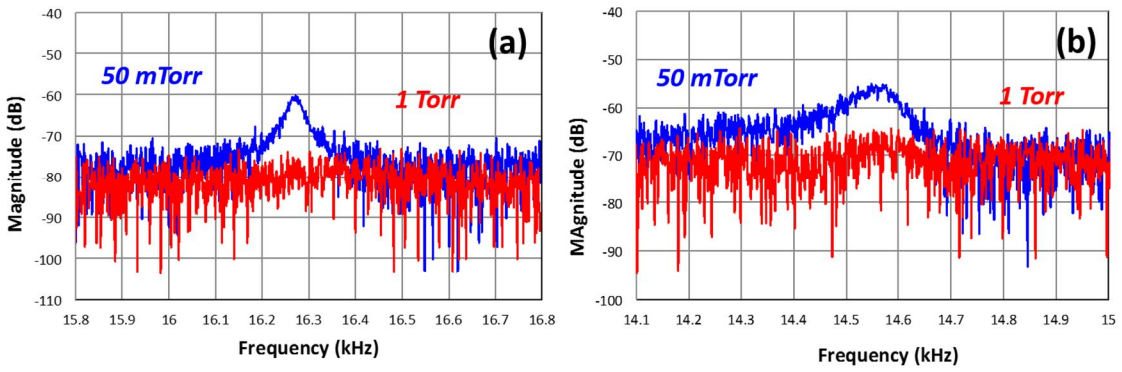


Figure 2. 29: Resonance response of *Gen-1* (a) in-plane and (b) out-of-plane accelerometer under different pressure level

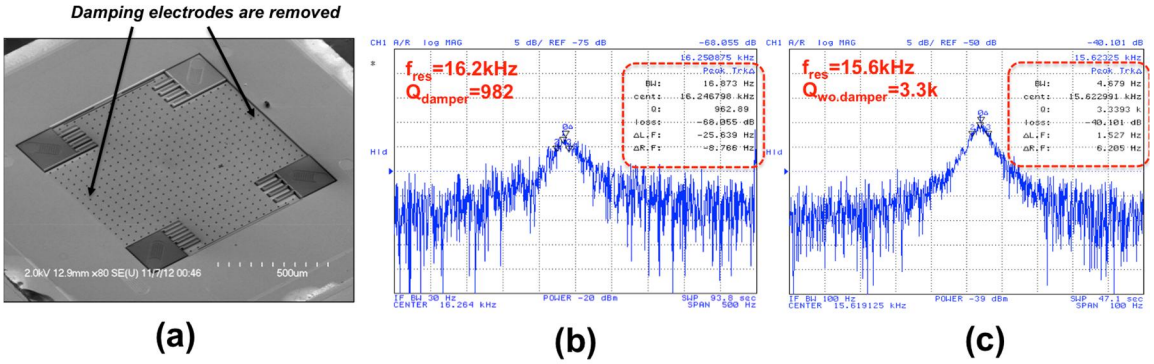


Figure 2. 30: (a) SEM photo of *Gen-1* in-plane accelerometer without damping electrode, and resonance response of (b) with and (c) without damping structure at 50 mTorr pressure

To fully-validate the effectiveness of using narrow gap on stability improvement, a separate in-plane accelerometer without the damping electrode is also implemented and its resonance response is plotted on Figure 2. 30. Measurement shows the accelerometer without damping electrode has higher quality factor *(Q)* compared to that of the original design *(3.3k VS 982)*. As other design geometry, such as the proof-mass, electrode and mechanical springs are identical to the original design, it is concluded that such difference in quality factor *(Q)* is solely caused by the existence of damping electrode.

The functionality of the capped device was verified by measuring the changing capacitance on sense electrode with respect to different bias voltage using Agilent 4285

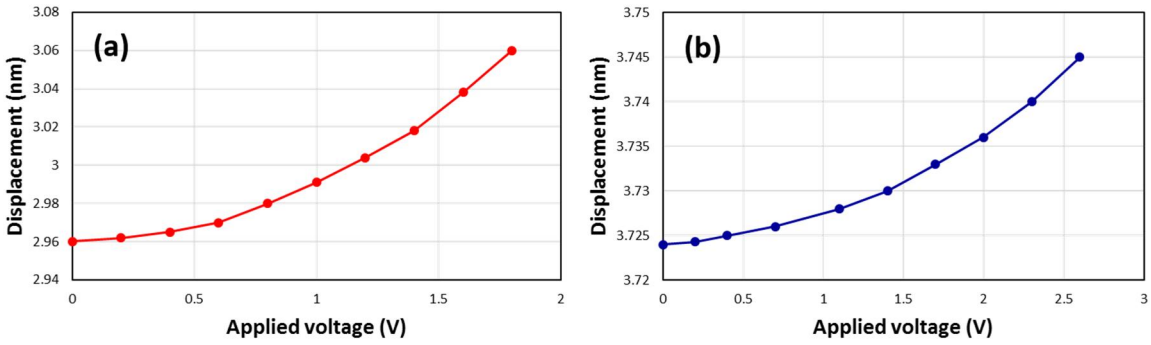


Figure 2. 31: *C-V* measurement of *Gen-1* (a) in-plane and (b) out-of-plane accelerometer

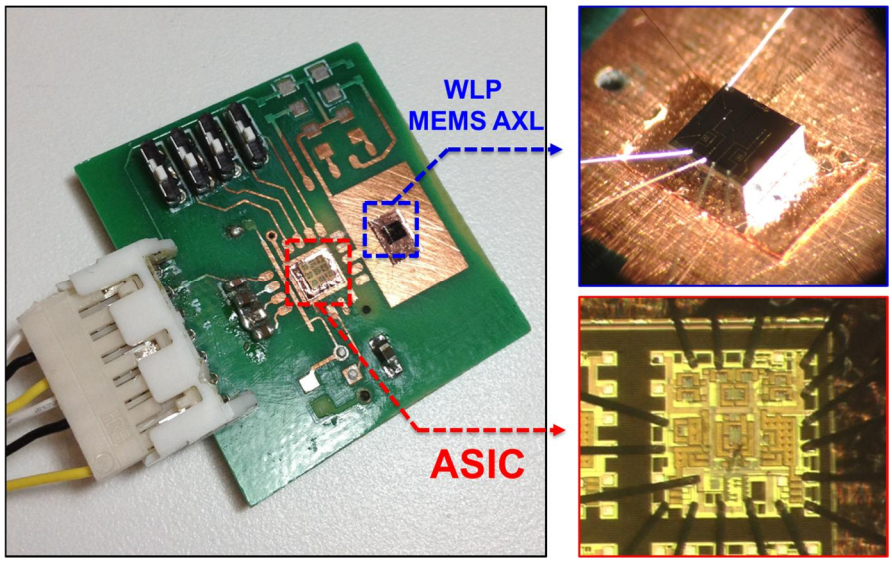


Figure 2. 32: Evaluation board with ASIC and wafer-level packaged *Gen-1* MEMS accelerometer interfaced via bond-wire

LCR meter. Induced electrostatic force attracts the proof-mass toward the electrode, which displacement is translated into a quadratic changing capacitance as shown on Figure 2. 31. Such behavior proves the functionality of wafer-level-packaged accelerometer.

The fabricated sensor is then wire-bonded to the readout ASIC as shown in Figure 2. 32. The readout ASIC is a switched capacitor circuit, which consecutively charges and discharge the MEMS capacitor to convert capacitance change into voltage. Its detailed operation will be discussed on Chapter 3. The output waveform of the interface circuit

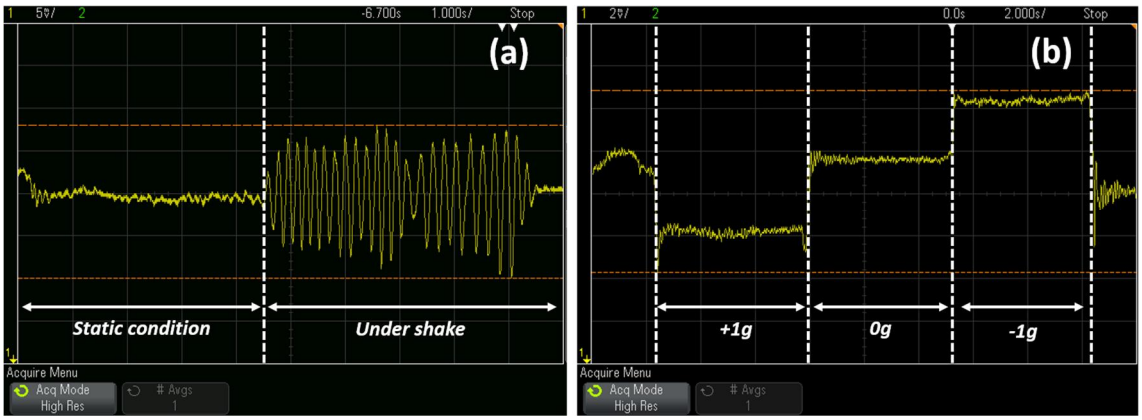


Figure 2. 33: Output waveform of the *Gen-1* accelerometer interfaced with ASIC when (a) external acceleration applied by the hand and at (b) +/- 1g tilting condition

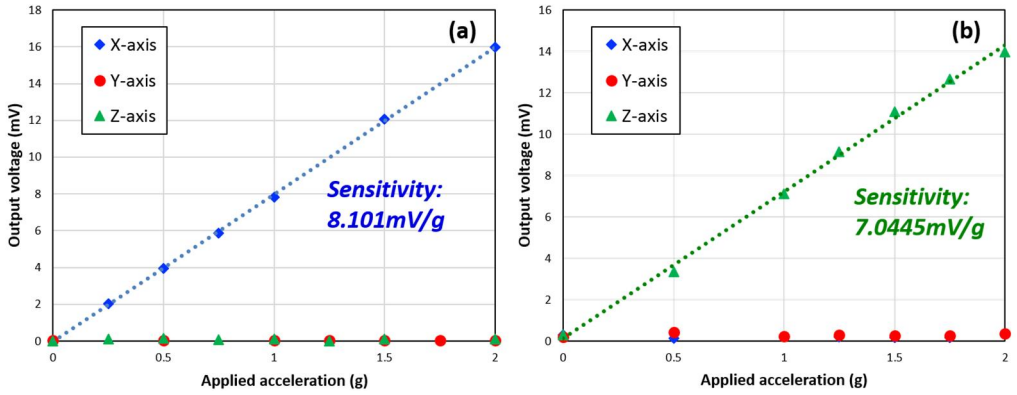


Figure 2. 34: Measured scale factor of *Gen-1* (a) in-plane and (b) out-of-plane accelerometer interfaced with readout circuit

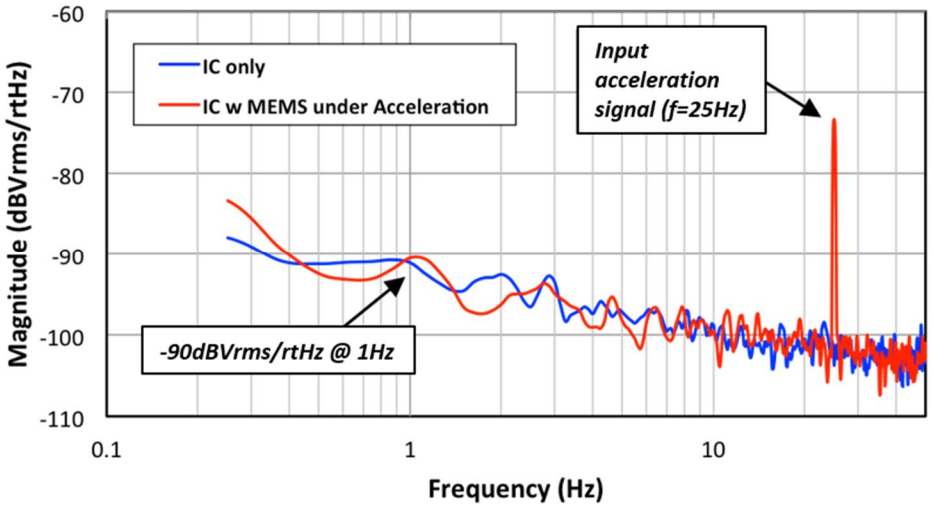


Figure 2. 35: Measured output noise spectrum of *Gen-1* MEMS accelerometer interfaced with readout electronics. ASIC-only configuration is also plotted in the same plot

under external acceleration and +/-1g tilting condition is shown at Figure 2. 33. It is clearly observable that even though fabricated accelerometer is operated under wafer-level packaged low-pressure environment (1~10 Torr), the output does not experience any instability behavior. The scale factor of the accelerometer is measured by attaching evaluation board to the shaker table and applying acceleration under *x*-, *y*-, and *z*- axis direction. Figure 2. 34 shows that in-plane and out-of-plane accelerometer has scale factor of 8.01 mV/g and 7.04 mV/g for out-of-plane accelerometer design respectively. Measured cross-axis sensitivity is 0.26 % for the in-plane and 0.42 % for the out-of-plane design, which are thought to be contributed by the alignment error between the evaluation board and the shaker, as the simulated values were less than 0.1%. Output noise performance at two different configurations (ASIC-only and ASIC+MEMS) were measured using Agilent 35670A dynamic signal analyzer. Figure 2. 35 shows that the electronics are the dominant source of noise as the measured spectrum between each configuration is similar each other. Measured noise density is about -90 $dBV_{rms}/\sqrt{Hz}$ at 1 Hz, which is equivalent to 3 to 4 $mg/\sqrt{Hz}$. Optimization on the interface circuit would improve the performance so that the entire noise is dominated by the Brownian noise. The measured performance summary of *Gen-1* in-plane and out-of-plane accelerometer are shown on Table 2. 3 [38]. It should be noted that by scaling down the gap size, the operational bandwidth of the accelerometer can be extended (f_{res}: ~ 15 kHz) while having sufficient capacitive sensitivity to ensure low-noise performance.

Table 2. 3: Performance summary of *Gen-1* Accelerometer

Parameter	In-plane design	Out-of-plane design
Proof-mass size	1 mm × 1 mm	
Device thickness	40 μm	
Capacitive gap size	300 nm	
Resonant frequency	Simulated: 13.647 kHz Measured: 16.2 kHz	Simulated: 16.761 kHz Measured: 14.5 kHz
Device Stiffness	468 N/m	610.7 N/m
Pull-in voltage	3.5 V	2.3 V
ΔC_S @ 1V	31 fF	5 fF
Static capacitance *(C_S)*	2.92 pF	3.73 pF
Simulated Quality factor *(Q)*	0.54 (10 Torr) / 6.92 (1 Torr)	0.923 (10 Torr) / 12.55 (1 Torr)
C/V gain	2.72 mV/fF (C_F=1.1pF)	
System scale factor	8.1 mV/g	7.04 mV/g
Capacitive sensitivity	Simulated: 6.32 fF/g Measured: 2.97 fF/g	Simulated: 12.3 fF/g Measured: 2.58 fF/g
Nonlinearity	0.31 % @ 2-g full-scale 0.45 % @ 6-g full-scale	0.91 % @ 2-g full-scale 1.3 % @ 6-g full-scale
Cross-axis sensitivity	S_{XY}: 0.26 % S_{XZ}: 0.112 %	S_{ZX}: 0.31 % S_{ZY}: 0.42 %
Noise density level @ 1Hz	-90 $dBV_{rms}/\sqrt{Hz}$ (3~4 $mg/\sqrt{Hz}$)	
Switching clock	200 kHz	

2.4. *GEN-2* ACCELEROMETER DESIGN

Characterization results on *Gen-1* design have proved the feasibility of employing sub-micron gap as a sensing electrode for quasi-static capacitive accelerometer and its effectiveness on extending bandwidth as well as enabling stable operation under low-pressure level. In this section, the *Gen-1* device is revised into the next version of design *(Gen-2)* aiming for precision performance as well as improved fabrication yield.

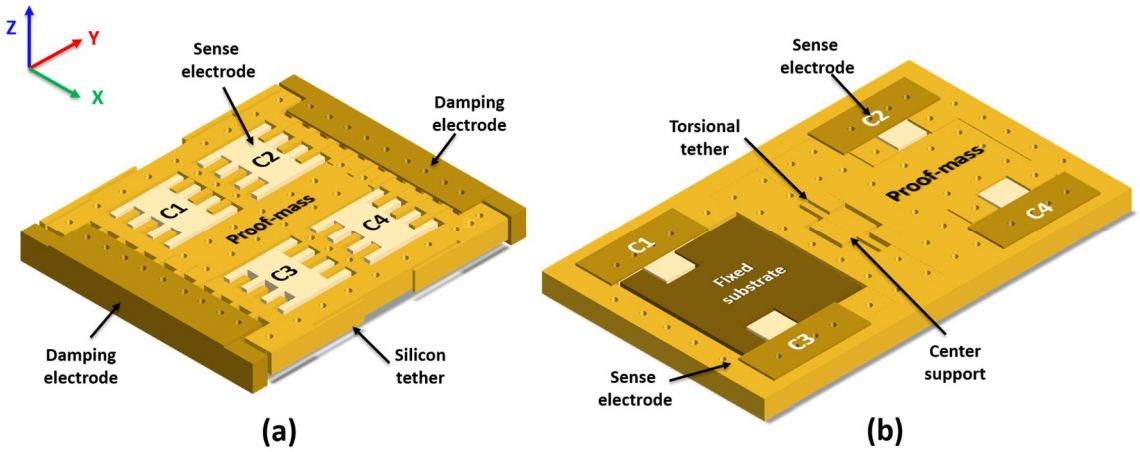


Figure 2. 36: Schematic diagram of (a) in-plane and (b) out-of-plane *Gen-2* accelerometer

Figure 2. 36 shows the schematic diagrams of *Gen-2* in-plane and out-of-plane accelerometer, which have number of modifications compared to initial *Gen-1* design. First, the lateral sensing gap is scaled down to 190 nm to increase the capacitive sensitivity as well as air-damping. Other device parameters such as stiffness or sensing area were adjusted accordingly to reflect such changes. Furthermore, the sensing fingers are placed at both sides of the four electrodes, which are relocated inside the proof-mass to maximize the sensing region per given area. It was observed that the poly-silicon tether used in *Gen-1* out-of-plane design experienced a larger process variation compared to single-crystalline silicon (SCS) springs, resulting in a poor fabrication yield. To address such issues, different

moving mechanism *(i.e. teeter-totter topology* [49]*)* is adopted to avoid use of poly-silicon tether. Figure 2. 36(b) shows the proposed *Gen-2* out-of-plane accelerometer, where the entire proof-mass is suspended by the torsional tether. A portion of the proof-mass from one side of the center support (-y) is intentionally removed to create a shift in center of mass. When the external acceleration is applied, such an imbalance creates a torque τ and creates the tilting movement as shown in Figure 2. 37.

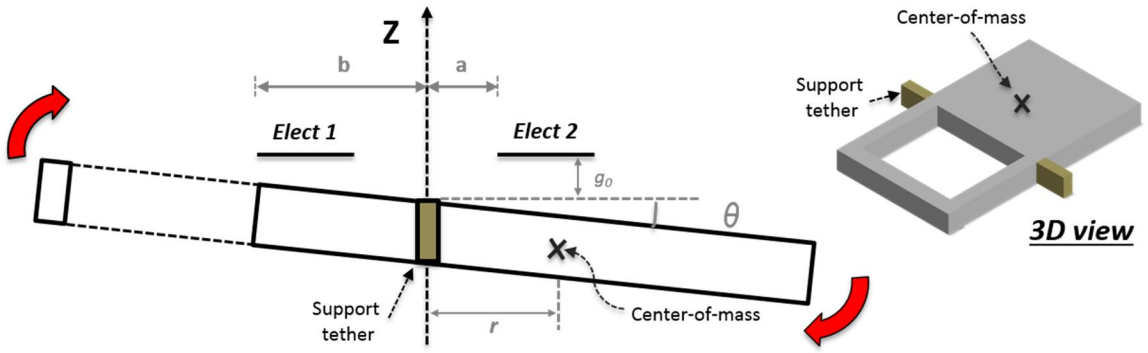


Figure 2. 37: Cross-section view of teeter-totter accelerometer movement under acceleration

Generated torque τ is expressed as equation (2-17), where r represents the distance of center-of-mass from the origin, and $K_{\theta.torsion}$ as rotational stiffness respectively. The silicon tether at center electrode behaves as a torsional spring, which rotational stiffness $K_{\theta.torsion}$ is expressed as equation (2-18). G stands for the shear modulus of the silicon, α represents the correction factor depending on the aspect ratio of the beam [50].

$$\tau = F_{accel} \cdot r = K_{\theta.torsion} \cdot \theta \quad (2\text{-}17)$$

$$K_{\theta.torsion} = \frac{4G\alpha h_t w_t^3}{l_t} \quad (2\text{-}18)$$

The rotated angle θ of the proof-mass is represented as equation (2-19), and resulting differential capacitance change ΔC is derived as equation (2-20). For the out-of-

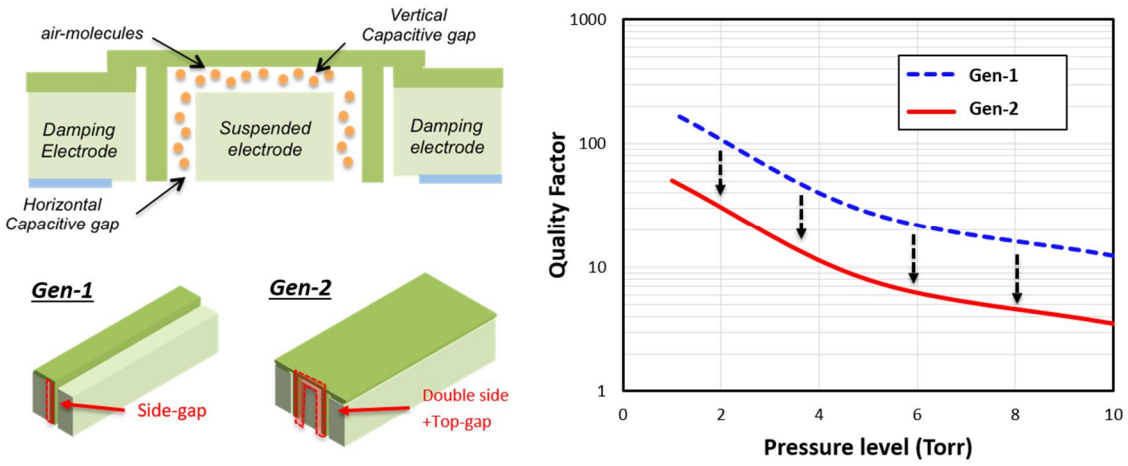


Figure 2. 38: (Left) Cross-section of damping electrode using both lateral and vertical gap (Right) Simulated Quality factor of each configuration respect to different pressure level

plane accelerometer shown in Figure 2. 36(b), the differential capacitance change would be equivalent to $\Delta C = C_1 - C_2 + C_3 - C_4$.

$$\theta = \frac{F_{accel} \cdot r}{K_{\theta.torsion}} = \frac{M \cdot r}{K_{\theta.torsion}} \vec{a}_{applied} \qquad (2\text{-}19)$$

$$\Delta C = C_+ - C_- = \int_a^{a+b} \left(\frac{\varepsilon_0 y_1}{g_0 - x \tan\theta} \right) dx - \int_a^{a+b} \left(\frac{\varepsilon_0 y_1}{g_0 + x \tan\theta} \right) dx \qquad (2\text{-}20)$$

Gen-2 design incorporates the improved version of damping electrode that utilizes both lateral and vertical sub-micron gap electrodes to attain increased squeezed-film-damping compared to *Gen-1* design without using additional area. This structure covers the entire damping electrode region using poly-silicon layer with vertical gap of 300 nm to bridge each finger as shown in Figure 2. 38. Doing so would trap any air-molecules that flows out from the lateral sub-micron gap electrode. FEM analysis using ANSYS simulator shows that by employing such revised scheme, the quality factor of the single beam reduces to 50.48 from 177.49 at pressure level of 1 Torr, which is close to 3 times of stability

improvement. Furthermore, as the separate fingers are bridged using poly-silicon layer, the device has increased stiffness, reducing the possibility of stiction [51].

2.4.1. SIMULATION ANALYSIS

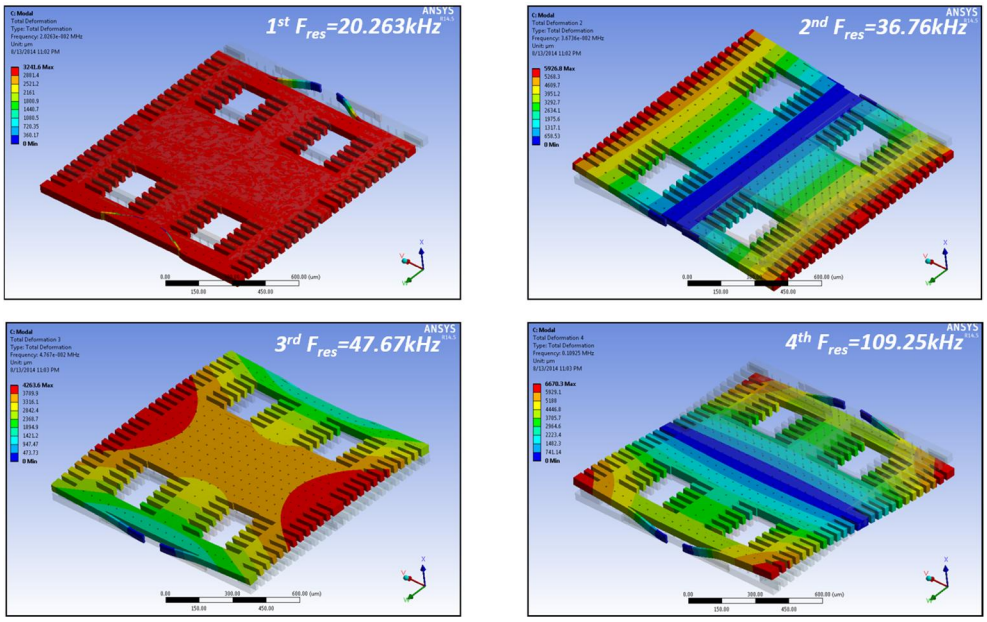


Figure 2. 39: Modal analysis of *Gen-2* in-plane accelerometer

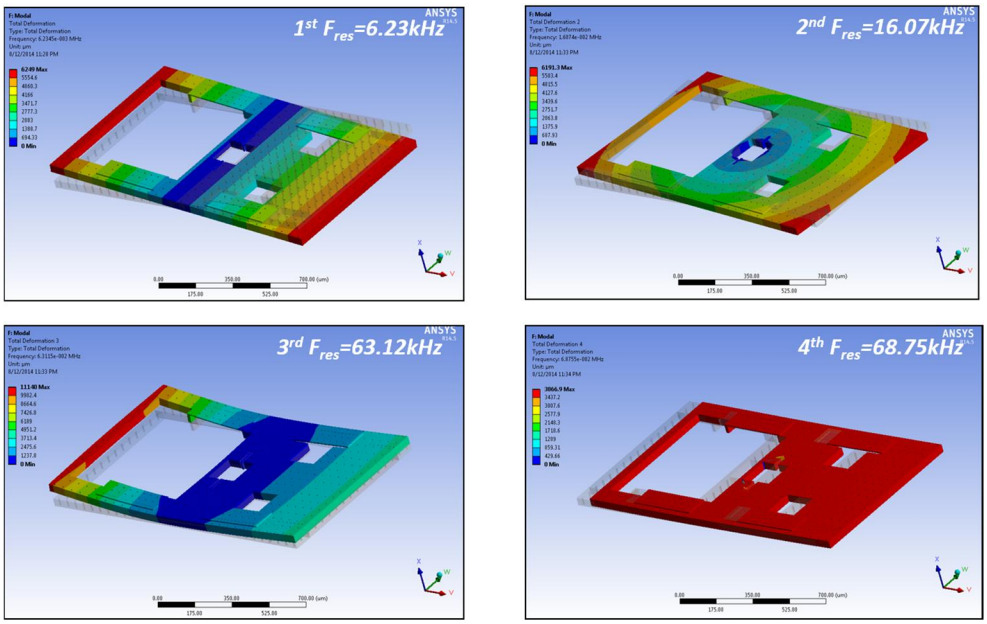


Figure 2. 40: Modal analysis of *Gen-2* out-of-plane accelerometer

Figure 2. 39 and Figure 2. 40 shows the modal analysis of the proposed *Gen-2* design. The resonant frequency of the in-plane accelerometer is 20.26 kHz, and out-of-plane design is 6.23 kHz. Similar to the *Gen-1* design, other parasitic modes ($2^{nd}/3^{rd}/4^{th}$) were intentionally made far higher than the dominant resonant mode to suppress unwanted coupling and to ensure robustness during fabrication.

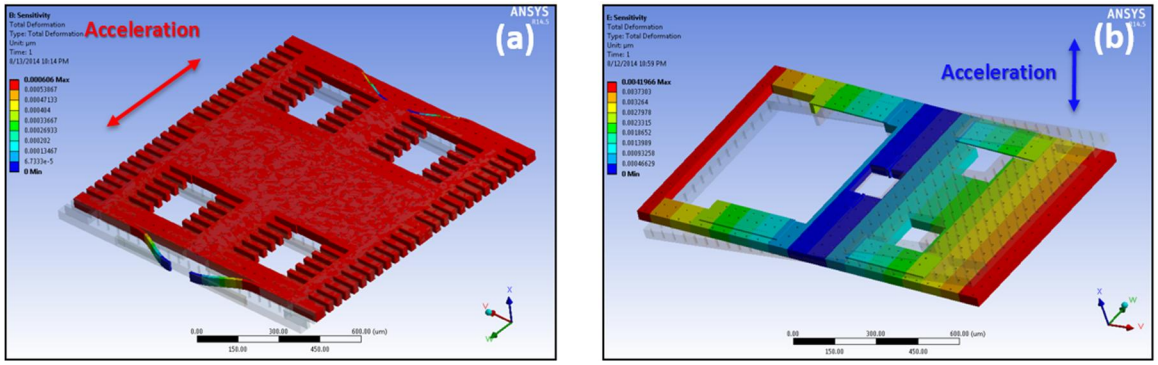


Figure 2. 41: Electrostatic simulation of *Gen-2* (a) in-plane and (b) out-of-plane accelerometer under 1 g acceleration

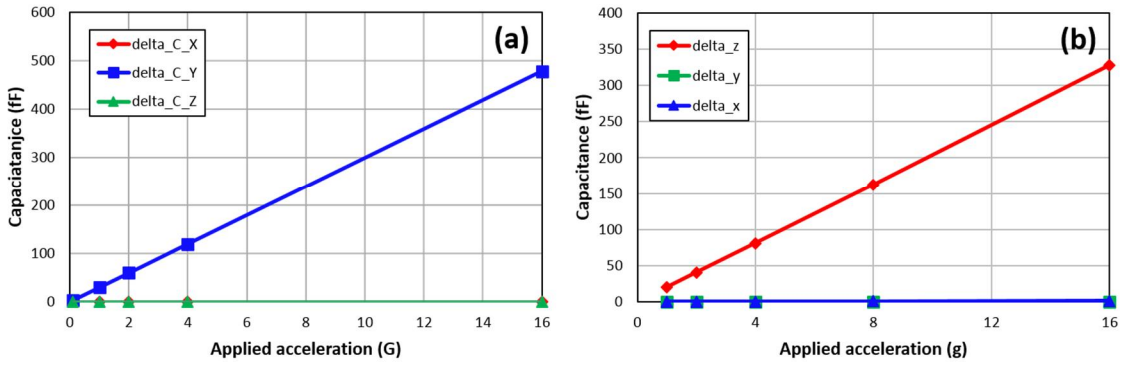


Figure 2. 42: Simulated scale factor of *Gen-2* (a) in-plane and (b) out-of-plane accelerometer

Figure 2. 41 and Figure 2. 42 shows the electrostatic analysis of the *Gen-2* accelerometer under 1-g acceleration, where the simulated scale factor is 29.9 fF/g for in-plane and 20.9 fF/g for out-of-plane design. The pull-in simulation at Figure 2. 43 shows 1.8 V and 2.1 V for each design respectively, which are still higher than the voltage difference between microstructure applied by the interface circuit ($V_{supply}/2$=1.25 V). The

simulated quality factor is 2.29 at 10 Torr and 33 at 1 Torr pressure level (Figure 2. 44). As the operating condition is slightly underdamped *(Q>0.707)*, each design will experience settling time of 146 µsec ~ 2.16 msec for in-plane and 462 µsec ~ 6.6 msec for out-of-plane design depending on the ambient pressure level. Using the worst-case settling time, the minimum system bandwidth performances are derived as 462.9 Hz for in-plane and 151.5 Hz for out-of-plane design respectively.

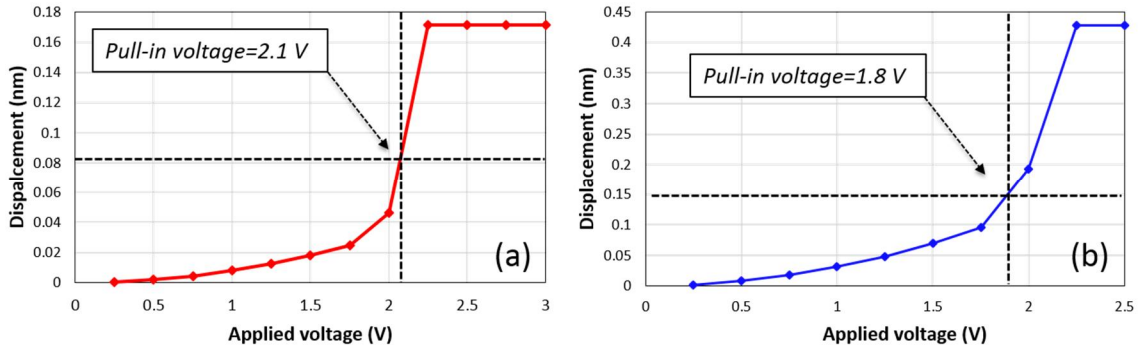


Figure 2. 43: Pull-in simulation result of *Gen-2* (a) in-plane and (b) out-of-plane accelerometer

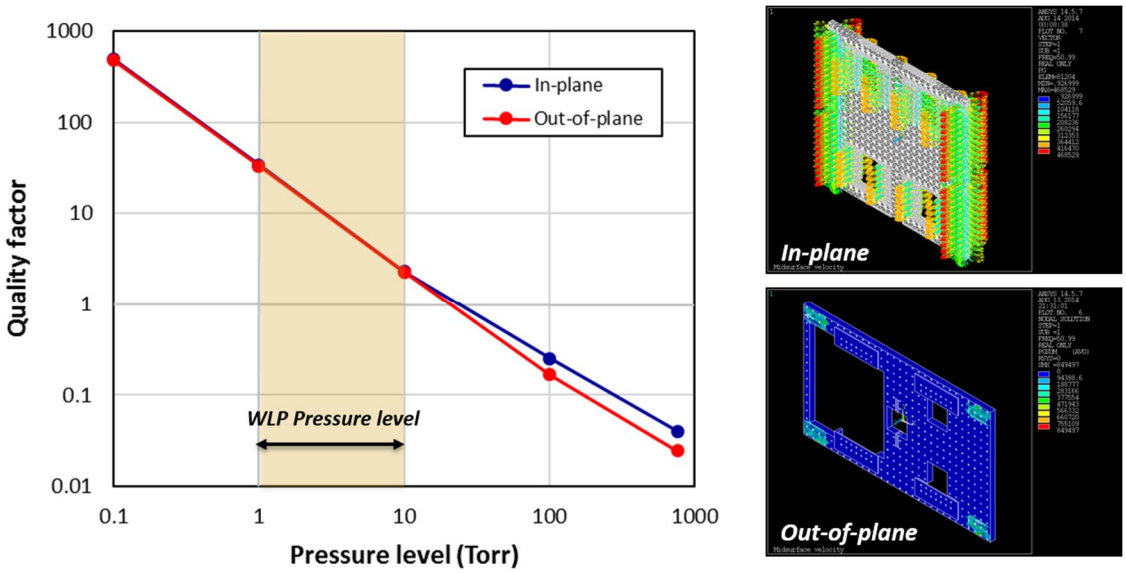


Figure 2. 44: Damping simulation result of *Gen-2* accelerometer

2.4.2. FABRICATION AND MEASUREMENT RESULT

Proposed accelerometer is fabricated on a 40 μm thick SOI substrate using HARPSS process [39][40] that was used to implement *Gen-1* design. The SEM photo of the acceleration sensor as well as other devices is shown on Figure 2. 45.

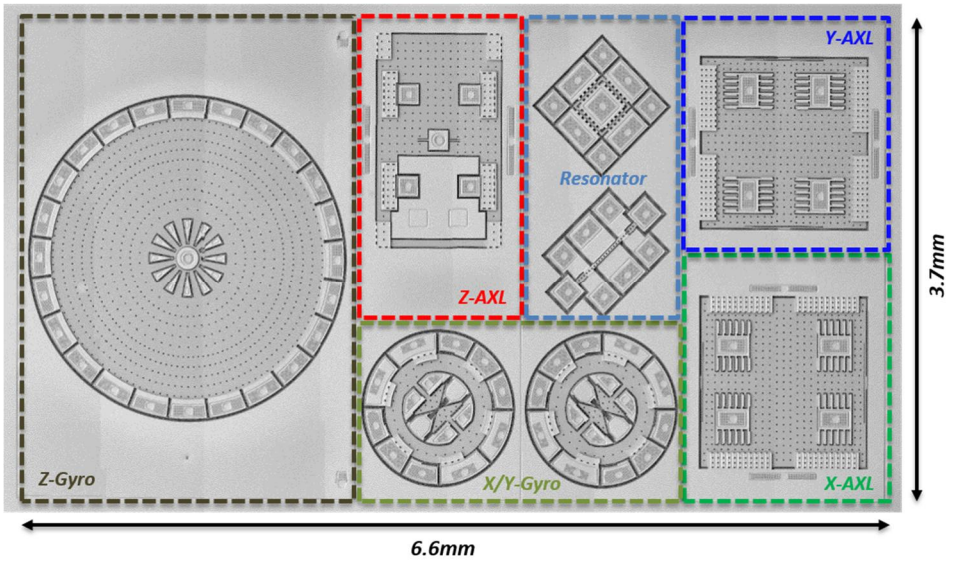


Figure 2. 45: SEM view of fabricated *Gen-2* accelerometer along with three-axis gyroscope and timing resonators

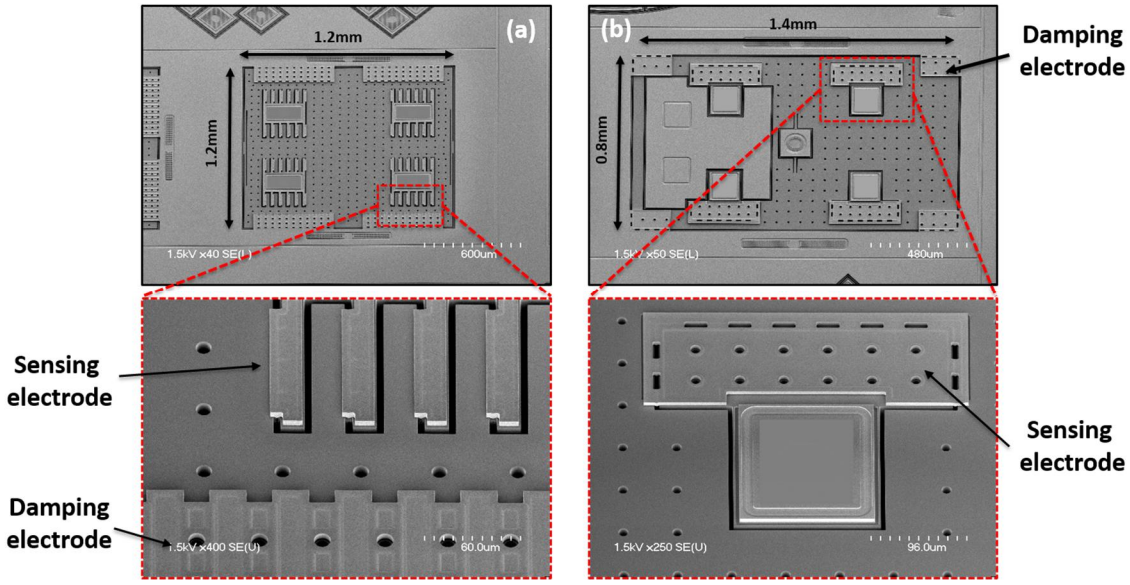


Figure 2. 46: SEM view of *Gen-2* (a) in-plane and (b) out-of-plane accelerometer and its closed-up view in sensing/damping electrode structure

Figure 2. 46(a) and (b) shows the SEM photo of in-plane and out-of-plane accelerometer. The entire device area including proof-mass and four sensing electrodes is equivalent to 1.2 mm × 1.2 mm for in-plane and 0.8 mm × 1.4 mm for out-of-plane design respectively. The closed-up view on in-plane accelerometer (Figure 2. 46(a)) clearly shows the poly-silicon layer that bridges the damping finger located at each side of the proof-mass. The sensing electrodes for out-of-plane accelerometer is attached to the proof-mass so that its gap size changes accordingly with respect to applied acceleration.

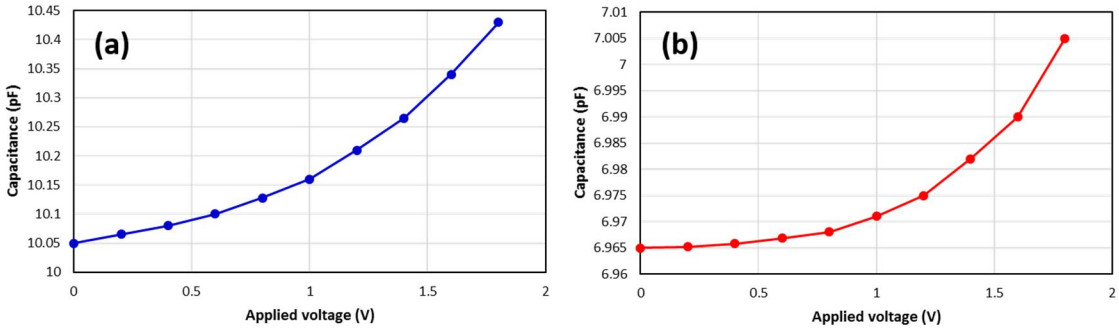


Figure 2. 47: C-V measurement of Gen-2 (a) in-plane and (b) out-of-plane accelerometer

After the wafer-level-packaging process, the functionality of both in-plane and out-of-plane accelerometer is verified through C-V measurement using Agilent 4284 LCR meter. The measured static capacitances were 5.25 pF for in-plane and 3.48 pF for out-of-plane design respectively. Figure 2. 47 shows quadratic relationship between the measured sense capacitance and the applied voltage, which validates the devices are functional. These devices are interfaced with readout electronics and underwent through characterization processes, where Figure 2. 48 shows measured output response under sinusoidal acceleration. Figure 2. 49 plots the measured scale-factor of in-plane and out-of-plane accelerometer. As the *Gen-2* devices have far higher capacitive sensitivity compared to that of *Gen-1*, improved performances were observed.

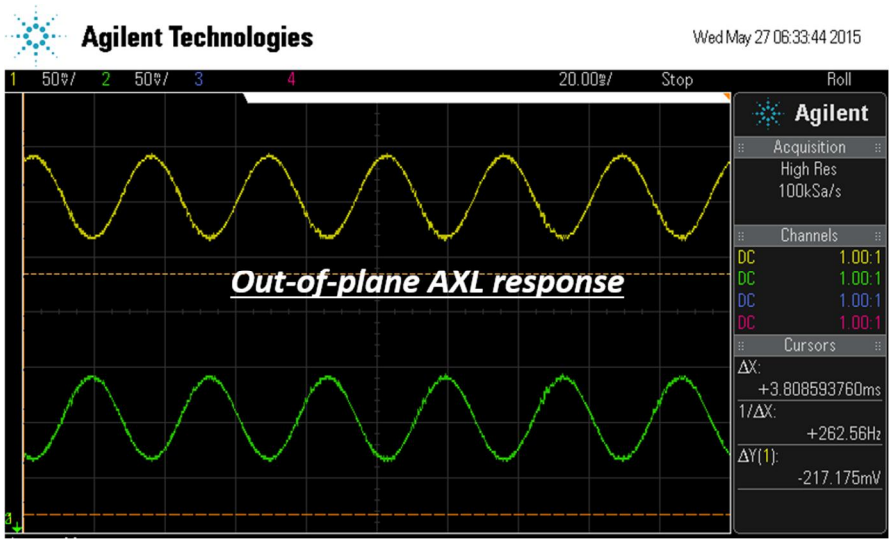


Figure 2. 48: Measured response of *Gen-2* out-of-plane design under sinusoidal acceleration

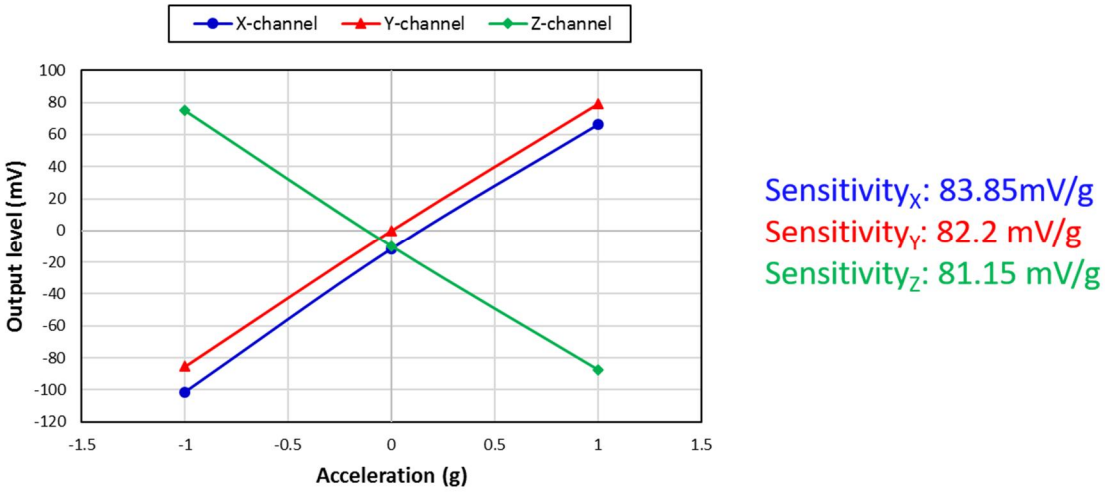


Figure 2. 49: Measured scale factor of *Gen-2* in-plane and out-of-plane accelerometer using +/-1-g tilt test

The measured noise spectrum of accelerometer is shown on Figure 2. 50, which suffers heavily due to the low-frequency noise This behavior is caused by the charging issue [52] of the thin nitride films that are incorporated on the MEMS electrode to protect box-oxide layer during release process. The detailed analysis on such phenomena will be presented at Chapter 4. Still, it should be noted that the measured noise level reduces drastically as the frequency increases. At 100 Hz, the noise floor gets close to thermal noise level, which in the range of 100 μg/√Hz.

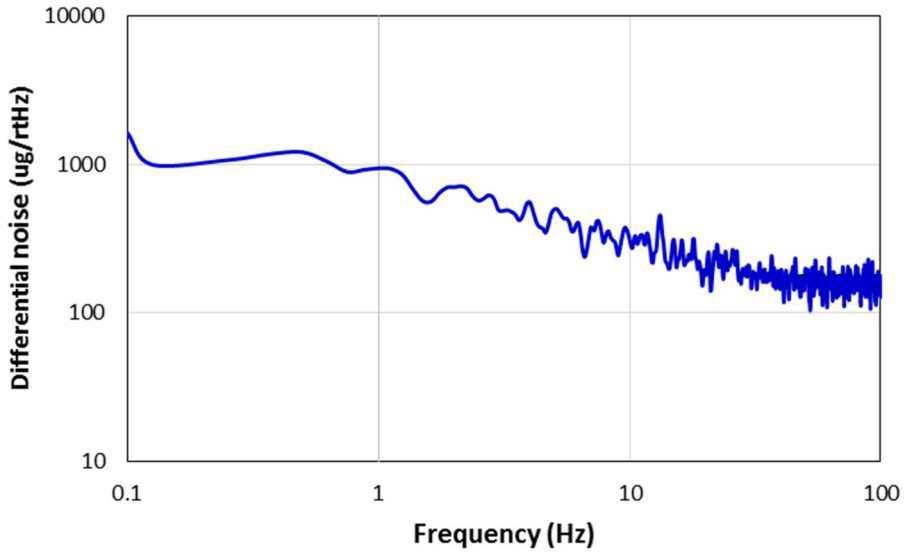


Figure 2. 50: Measured noise spectrum of *Gen-2* MEMS accelerometer interfaced with circuit

Table 2. 4: Performance summary of *Gen-2* accelerometer

Parameter	In-plane design	Out-of-plane design
Proof-mass size	1.2 mm × 1.2 mm	1.4 mm × 0.8 mm
Device thickness	40 µm	40 µm
Capacitive gap size	190 nm	300 nm
Resonant frequency	20.263 kHz	6.23 kHz
Device Stiffness	1542.68 N/m	39.28 N/rad (Rotational)
Capacitive sensitivity	29.9 fF/g	20.9 fF/g
Pull-in voltage	1.8 V	2.1 V
ΔC @ 1V	90 fF	6 fF
Quality factor *(Q)*	2.3 (10 Torr) 34 (1 Torr)	2.29 (10 Torr) 33 (1 Torr)
Sensitivity	83.85 mV/g	81.15 mV/g
Resolution level	~ 100 µg/√Hz @ 100 Hz	

2.5. SLOPED-ELECTRODE IN-PLANE ACCELEROMETER

2.5.1. DESIGN METHODOLOGY

Shock protection is one of the critical features in accelerometer design as the sensor often experiences an extreme shock that exceeds the input range of the device. Table 2. 5 summarizes a list of acceleration magnitudes that occur during daily life.

Table 2. 5: List of acceleration magnitude under various situation

Magnitude	Description
1 g	Standard gravity
3 - 6 g	High-g roller coaster [53]
100 g	Automobile crash [54]
300 g	Soccer ball struck by foot
3000 g	Baseball struck by bat [55]
> 5000 g	Shock capability of mechanical watches [56]
15,000 g	Firing from artillery shells [57]

When the high-g acceleration (>1,000 g) is applied, the proof-mass undergoes a large displacement that ultimately increases the generated strain at the mechanical spring. If the generated stress is higher than the fragile limit of the silicon (~1 GPa) [58], the microstructure would crack or completely break. Also, when the proof-mass makes a direct contact with the sensing electrode, number of small particles are generated, resulting in electrical short when interfaced with readout electronics. To prevent such catastrophes, majority of accelerometers are equipped with shock stop, or over-range stop structure [59]. The shock stop structure has smaller gap size than the sensing electrode (Figure 2. 51), so that it can block the excessive movement of proof-mass when high-g acceleration is applied. As the movement of the proof-mass is limited by the shock stop, generated stress does not

exceed the fragile limit of the silicon, making the design less immune to extreme environment. Even if micro-particles are generated between microstructures, they are only generated near the shock stop region. As both shock stop and the proof-mass is biased at the same electrical potential, generated particles would not create electrical problems when interfaced with electronics.

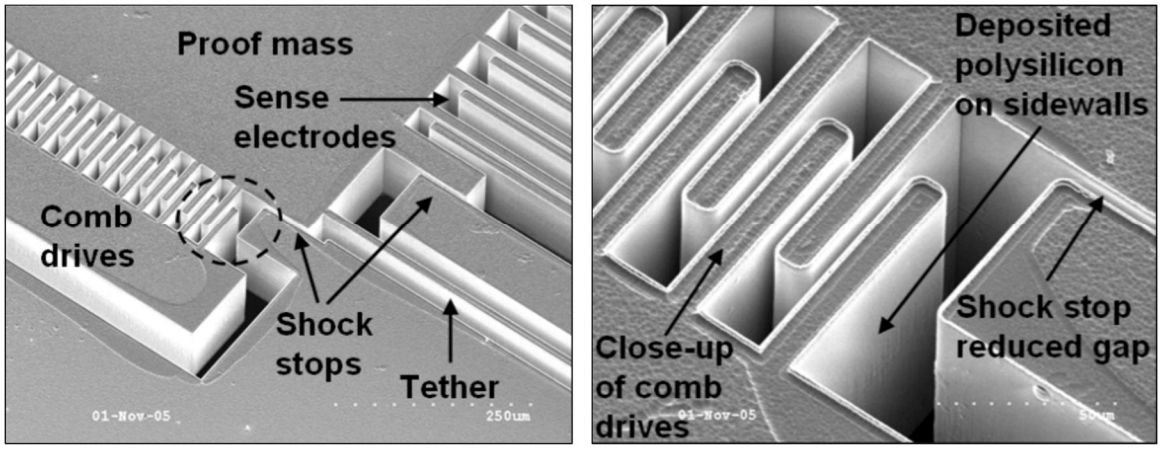


Figure 2. 51: SEM view of implemented shock stops on accelerometer [12]

As the proposed accelerometer has higher resonant frequency compared to the conventional design, amount of generated stress is relatively small and does not exceed the fragile limit of the silicon. Figure 2. 52 shows the simulated *Gen-2* in-plane accelerometer movements under 15,000 g acceleration from three different axes *(X-/Y-/Z-)*. As the amount of generated stress (~100 MPa) is well below the fragile limit (~1 GPa) [58], it can be concluded that the sensor would be intact even under extreme shock condition. However, the proof-mass still makes a direct contact with the sense electrode during high-g acceleration, which may create micro-particle and result in electrical short problem when interfaced with the readout electronics.

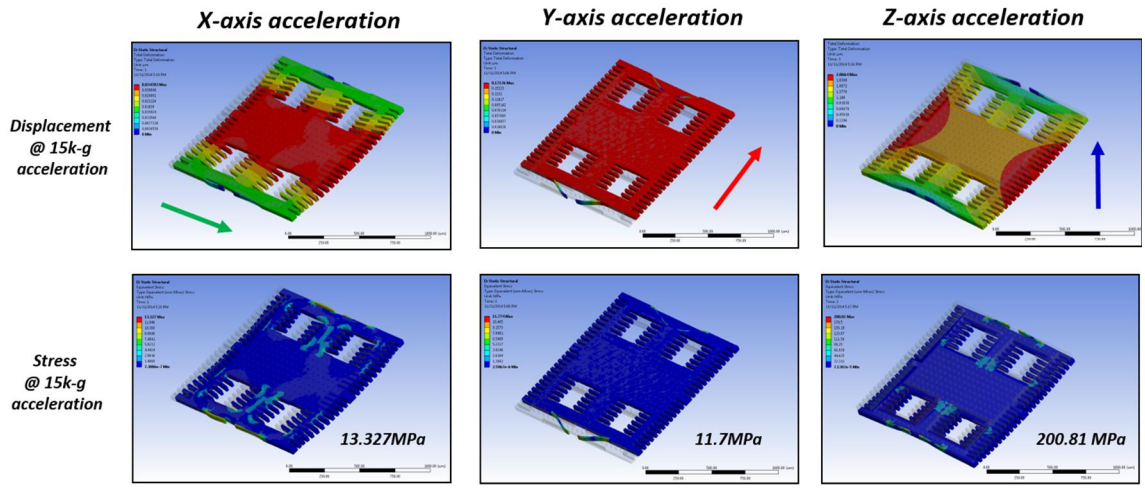


Figure 2. 52: Simulated displacement and generated stress of in-plane accelerometer under 15,000 g acceleration from three different axes *(X-/Y-/Z-)*

Although this problem can be easily solved by incorporating shock stop structure, the fact that proposed accelerometer is not implemented using standard MEMS fabrication process complicates the task. Whereas most of MEMS sensors are fabricated using DRIE process that employs optical lithography, proposed accelerometers utilize specific fabrication process that uses sacrificial layer to create high aspect ratio sub-micron sensing gap [39] as shown in Figure 2. 53(b). To implement multiple different sub-micron gap sizes, one requires increased number of photomasks and fabrication steps as the thickness of the sacrificial layer is uniform across the entire wafer.

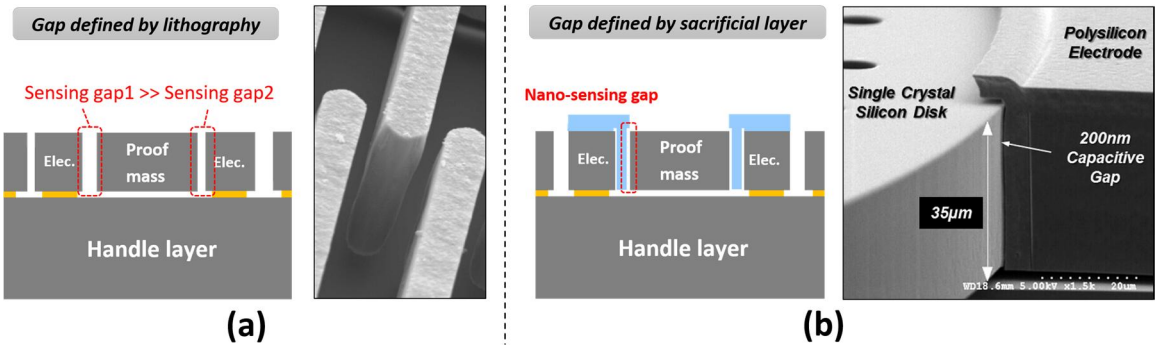


Figure 2. 53: Comparison between MEMS devices fabricated using (a) conventional DRIE process defined by optical lithography and (b) HARPSS process using sacrificial layer

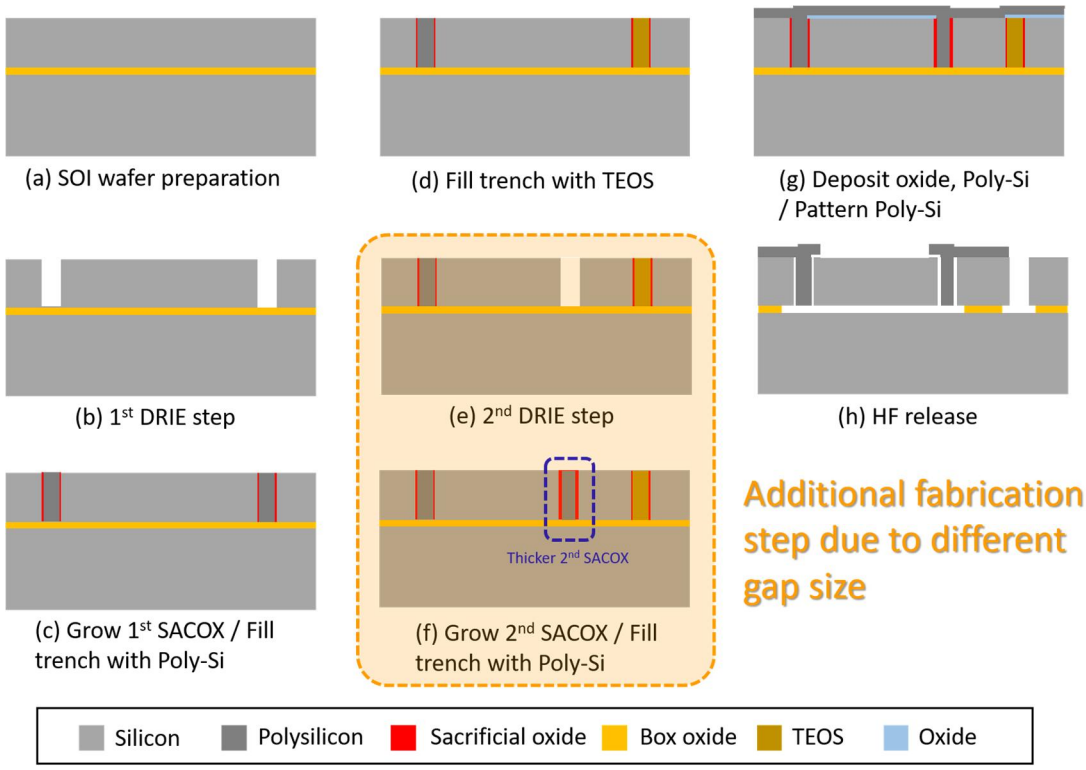


Figure 2. 54: HARPSS fabrication diagram of MEMS accelerometer having dual sub-micron sensing gap; Additional fabrication step to implement another gap size is highlighted

This problem is further explained in Figure 2. 54, which shows the overall fabrication processes that enables implementing different sub-micron gap sizes. As can be seen from the figures, additional photomasks as well as separate processing steps are required to define the region with different thickness sacrificial layer. As doing so ultimately raises the overall fabrication cost, time, and production yield, the implementation of shock stop becomes a costly chose.

To address such problem, a novel sloped electrode, which schematic diagram is shown on Figure 2. 55 is proposed in this dissertation [60]. Compared to conventional parallel-plate electrode, this configuration employs interdigitated fingers that are tilted so that its normal vector is at angle θ with respect to the device motion. Assuming the device

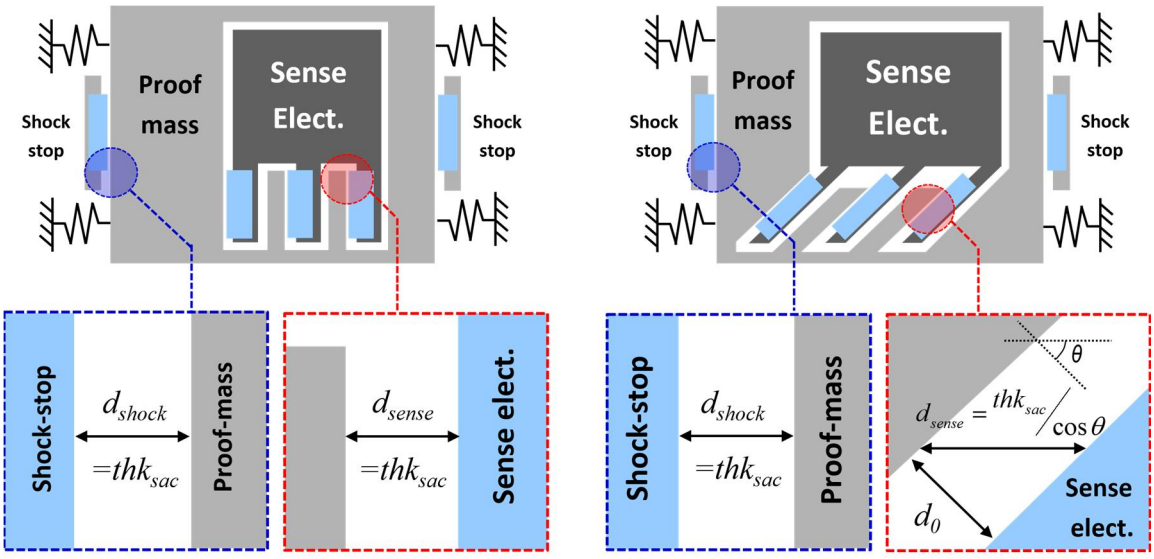


Figure 2. 55: Comparison between (Left) parallel-plate and (Right) sloped electrode

moves only along *X*- axis on Figure 2. 55, the required travelling distance to make contact with the sense electrode (i.e., effective gap) can be derived as equation (2-21), where thk_{sac} is the sacrificial layer thickness.

$$d_{\text{effective}} = \frac{thk_{sac}}{\cos\theta} \qquad (2\text{-}21)$$

Even if the sacrificial layer thickness tck_{sac} is constant over the entire device (single deposition), equation (2-21) shows that different effective gap sizes are still attainable by changing the angle θ on the electrode. For the region that requires minimum gap (i.e., shock stop), the microstructure can be designed so that its normal vector is parallel with the device motion. On the other hand, for the sensing regions, where larger gap is needed, the angle θ can be increased to widen the effective travelling distance of the proof-mass.

Sloping the sensing finger would deteriorate the capacitive sensitivity of the accelerometer as it increases the effective sensing gap of the device. For example, if the normal vector of sloped finger is 90 degrees with the sensitive axis, the sense electrode of

accelerometer would become a comb-sensing, which the sensitivity is orders of magnitude smaller than parallel plate sensing. Overall the capacitive sensitivity on the sloped electrode follows the combination between parallel-plate *(θ=0°)* and comb-finger *(θ=90°)* sensing configurations as shown in equation (2-22)

$$\frac{\Delta C}{\vec{a}} \approx \frac{2\varepsilon_0 N_e H}{\omega_0{}^2 d} \cdot \left(\frac{l_e}{d} \cos\theta_e + \sin\theta_e \right) \qquad (2\text{-}22)$$

Such reduction in capacitive sensitivity can be compensated by increasing the electrode length l_e, or lowering the resonant frequency ω_0 of the device. It should be noted that there will be minor loss on the proof-mass while increasing the electrode length l_e.

2.5.1. MEASUREMENT RESULT

The proposed sloped electrode configuration is incorporated into the accelerometer design as a proof-of-concept and fabricated using HARPSS process [39] on a 40 μm thick SOI substrate as shown on Figure 2. 56. This device is consecutively wafer-level packaged and interfaced with readout ASIC as shown in Figure 2. 57. The size of entire die, including sealing ring and related electrodes is 2 mm × 2mm. Considering the target thickness of sacrificial oxide layer is 270 nm and the sensing electrode has 45 º angle with the proof-mass movement, the effective sensing gap becomes 381.8 nm. On the other hand, the normal angle of the shock stop structures that are located each end of the proof-mass is parallel with the device movement, resulting an effective gap size of 270 nm, which is sufficient to prevent excessive device movement under high-g acceleration. As the presented design is operated under wafer-level-packaged low-pressure environment (1~10 Torr), the damping electrode [38], which angle is 15 º with respect to device movement is

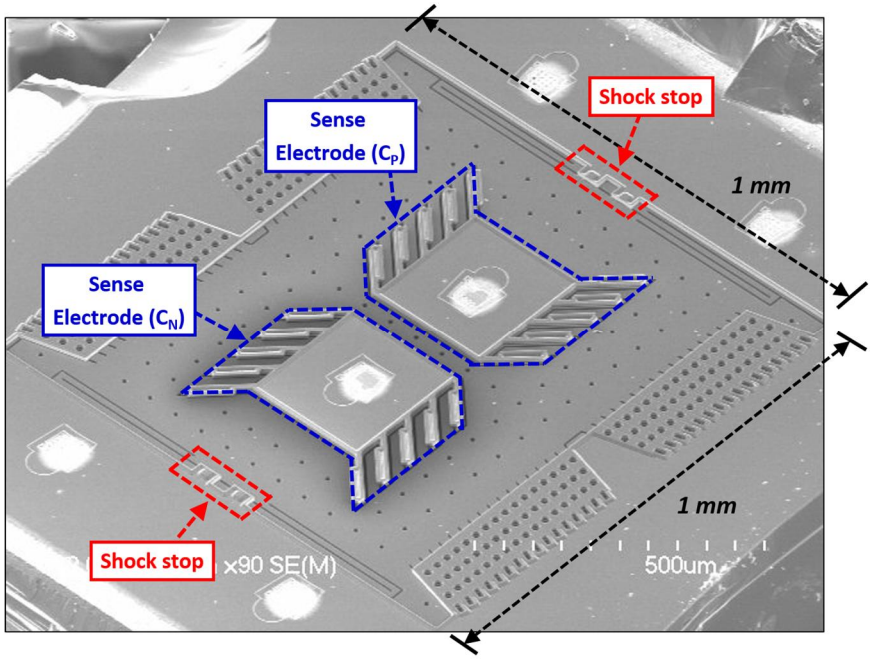


Figure 2. 56: SEM microphotograph fabricated MEMS in-plane accelerometer, incorporating sloped electrode configuration to extend effective sensing gap size

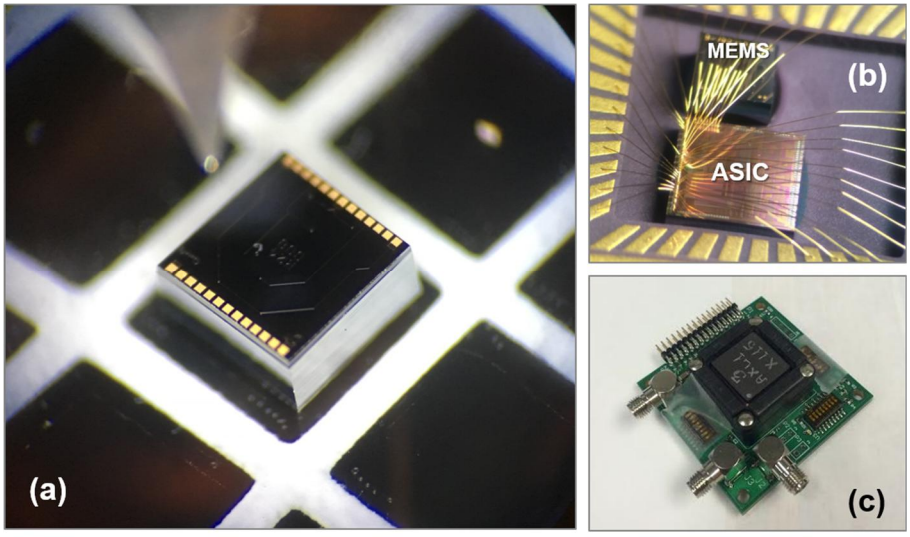


Figure 2. 57: Microphotograph of (a) wafer-level packaged accelerometer, (b) device interfaced with readout ASIC, and (c) evaluation board

also added to provide sufficient air-damping. Figure 2. 59 and Figure 2. 58 shows the closed-up SEM and IR microphotograph of sloped sensing electrode and shock stop. The shock stop is a *"U-shaped"* structure that is covered with poly-silicon layer so that its normal vector on each plane is parallel with all three axes *(X/Y/Z-axis)*. Doing so sets the

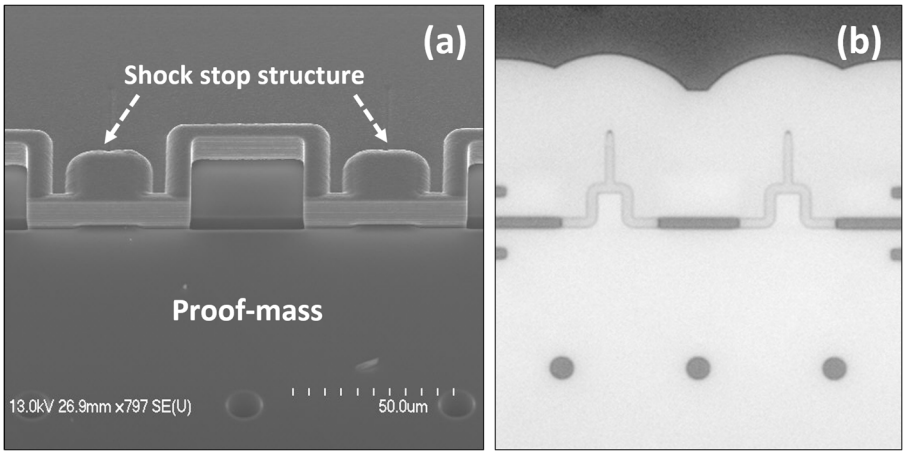


Figure 2. 58: (a) SEM and (b) IR (Infra-red) microphotograph shock stop structure

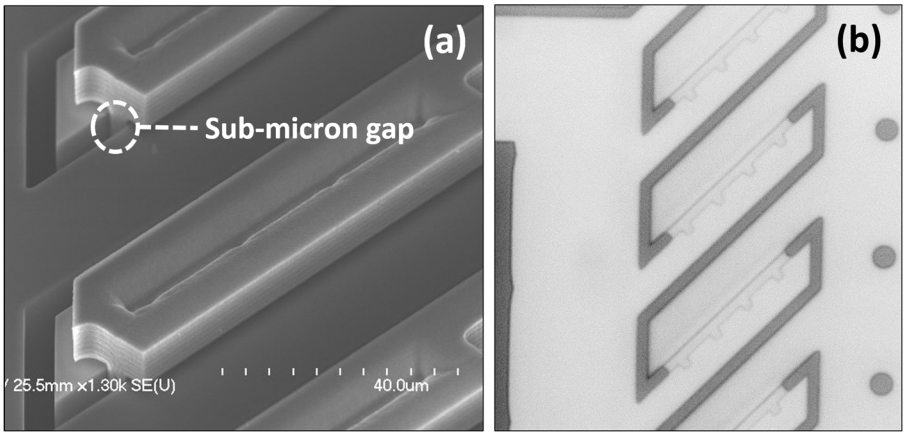


Figure 2. 59: (a) SEM and (b) IR (Infra-red) microphotograph of sloped sensing electrode

effective gap size equivalent to sacrificial layer thickness *(thk_{ox})*, providing shock protection on all directions.

The functionality of the accelerometer was first verified by measuring its resonant response by placing an uncapped MEMS device inside the vacuum chamber, where one of sense electrodes were used as an actuation port and the other was connected to the readout channel of network analyzer. The proof-mass was biased with constant polarization voltage to generate a sufficient electrostatic force. When the pressure level inside the chamber was pulled down to less than 50 mTorr, the number of air-molecules becomes so scarce that the

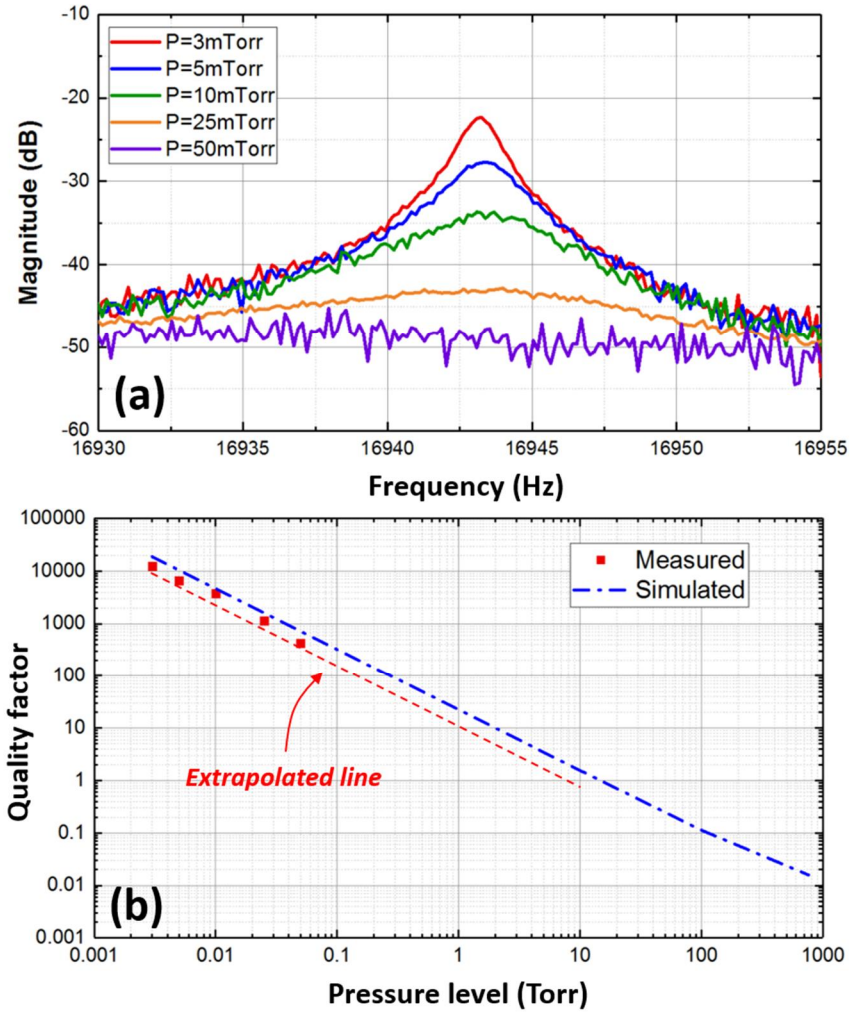


Figure 2. 60: (a) Measured resonant response of the accelerometer (b) Comparison between measured and simulated Q with different pressure level

effect of D_{SFD} gets negligible, and the resonant behavior starts to appear as Figure 2. 60(a). Measured resonance peak is at 16.94 kHz. The high-Q response diminishes when the pressure level increases more than 50 mTorr due to increased air-damping. Considering the pressure level inside the WLP environment is between 1 to 10 Torr, such measurement validates the stability of the wafer-level vacuum-packaged accelerometer. Measured quality factor from the resonant response was plotted with respect to different pressure level on Figure 2. 60(b). By extrapolation, it is concluded that the quality factor of the device would reach between 0.8 to 9.4 at wafer-level vacuum-packaged environment (1~10

Torr). The device may operate under slightly under-damped condition, but the resulting instability behavior is negligible enough not to affect the sensor performance, as the maximum device displacement at 16 g acceleration due to overshoot is 25.57 nm (7 % of effective gap).

The sensor was interfaced with a switched capacitor (SC) application specific integrated circuit (ASIC), which is fabricated using TSMC 0.13 μm process. The evaluation board shown on Figure 2. 57(c) is mounted on a ET-126 shaker table and underwent through 50 Hz sinusoidal accelerations as large as ± 16 g in all three-axis *(X/Y/Z-axis)* directions. The output tone of the readout circuit is measured using Agilent 35670A dynamic signal analyzer and plotted on Figure 2. 61(a). The cross-axis sensitivities are measured at 0.76 % (S_{XY}) and 1.26 % (S_{XZ}), which are thought to be caused by the alignment error between the device and the shaker table as the simulated cross-axis sensitivity was less than 0.1 % for all axis. The measured non-linearity of the scale factor was 0.8 % (= ± 0.4 %) at a full-scale range of 16 g (Figure 2. 61(b)), which can be improved by using a centrifuge setup, which suffers less parasitic vibration compared to shaker table by applying constant acceleration. Doing so would enhance the nonlinearity performance close to simulated value, which is less than ± 0.1 % at 16 g full scale range.

The noise performance is evaluated using Agilent 35670A dynamic signal analyzer and plotted on Figure 2. 61(c), showing 221 μg/√Hz at 1 Hz, and remains flat over the entire frequency bandwidth up to 50 Hz. These results show significant improvement compared to the previously reported work [11]. The measured Allan deviation plot of the accelerometer is shown in Figure 2. 61(d), exhibiting a bias instability of 177.8 μg and

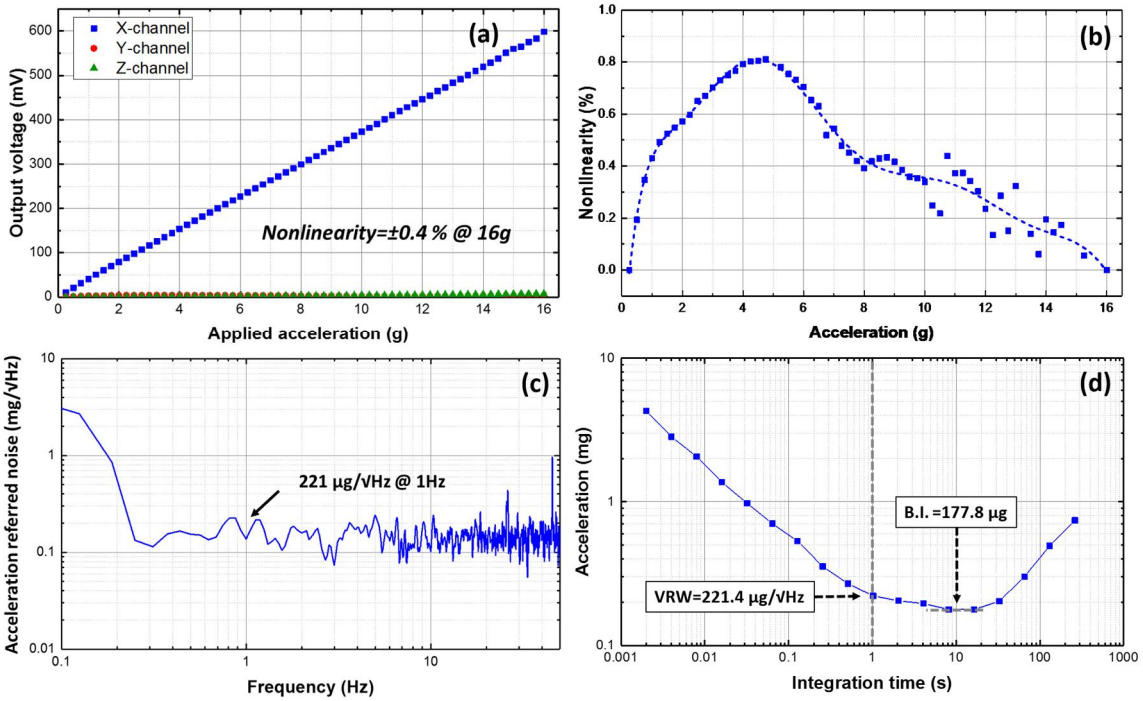


Figure 2. 61: Measured (a) scale factor with respect to three different axes of acceleration, (b) non-linearity (c) noise density level and (d) Allan deviation plot of MEMS accelerometer

velocity random walk (VRW) of 221.4 µg/√Hz. The resolution of the accelerometer is currently limited by the noise of the readout ASIC.

The operational bandwidth of the accelerometers was verified using ET-126 shaker table, which has capability to apply acceleration with different excitation frequencies from DC to 8.5 kHz. For fair comparison, commercial accelerometer (ADXL335) [24] has also undergone through same measurement and the bandwidth was compared as Figure 2. 62. Whereas the commercial accelerometer shows 3-dB cutoff frequency near 2 kHz, the output response of presented accelerometer remains flat up to 8.5 kHz. Such behaviors were enabled by the high resonant frequency (~15 kHz) nature of the microstructure.

The stability of WLP accelerometer was evaluated by applying a sudden shock (t=15 ms) and observing its output settling to the original level. The commercial

accelerometer ADXL335 [24] was also undergone through the same measurement for fair comparison. The output waveform on Figure 2. 63 shows that the both sensors experiences similar settling time of 600 ~ 800 msec, which is caused by the measurement setup, but not by the sensor itself. The fact that the output of accelerometer follows similar response as the commercial device indicates its operation does not experience instability issues.

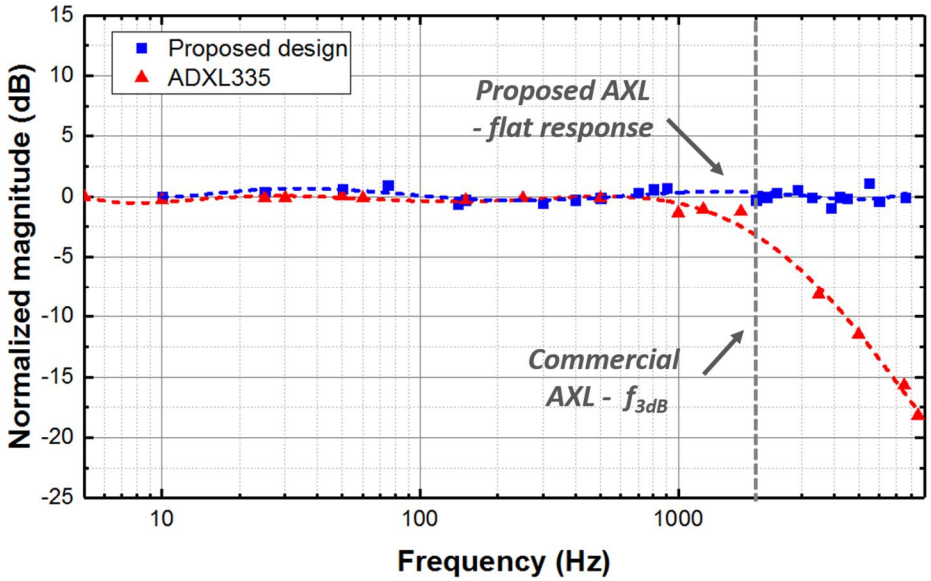


Figure 2. 62: Measured operational bandwidth of MEMS accelerometer and commercial product (ADXL335)

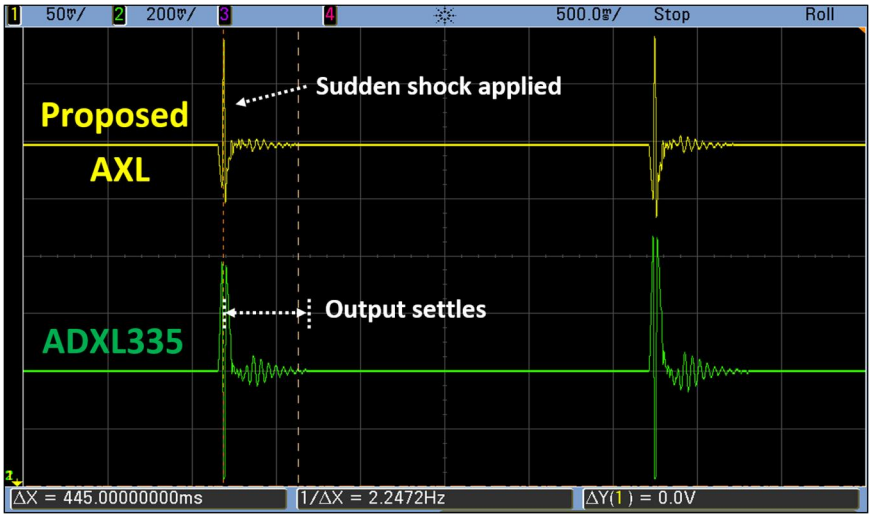


Figure 2. 63: Measured step response of MEMS accelerometer under sudden shock *(t=15 ms)*

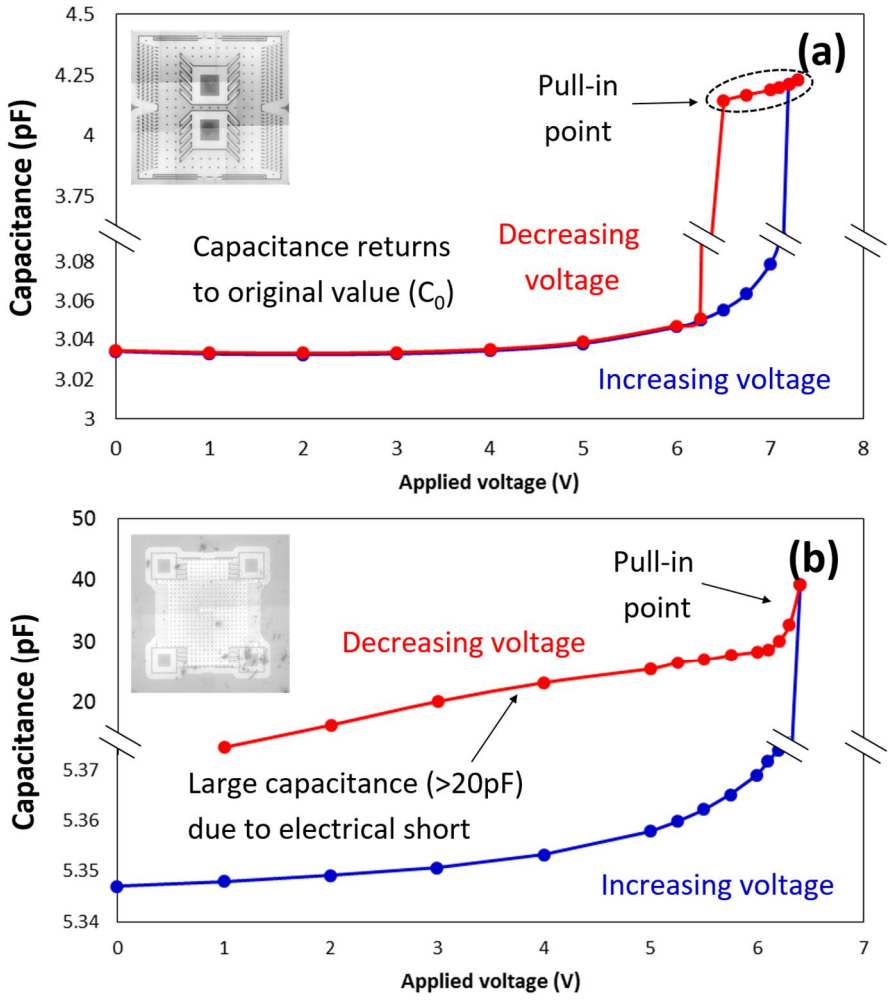


Figure 2. 64: Pull-in behavior of accelerometer (a) with and (b) without sloped electrode

Number of different characterizations were conducted to verify the effectiveness of the sloped electrode design. First, different polarization voltages (V_P) were applied on the device, to mimic the extreme shock condition by creating an intentional pull-in, and its MEMS capacitance was plotted as shown on Figure 2. 64. Figure 2. 64(a) shows that the MEMS capacitance of the sloped-sensing electrode returns to initial value (C_0) as the excessive proof-mass movement is blocked by the shock stop. However, when the accelerometer does not use the sloped sensing electrode, the intentional pull-in results in electrical short between microstructures, which causes MEMS capacitance not returning to its initial value (C_0) even when the V_P is not applied (Figure 2. 64(b)).

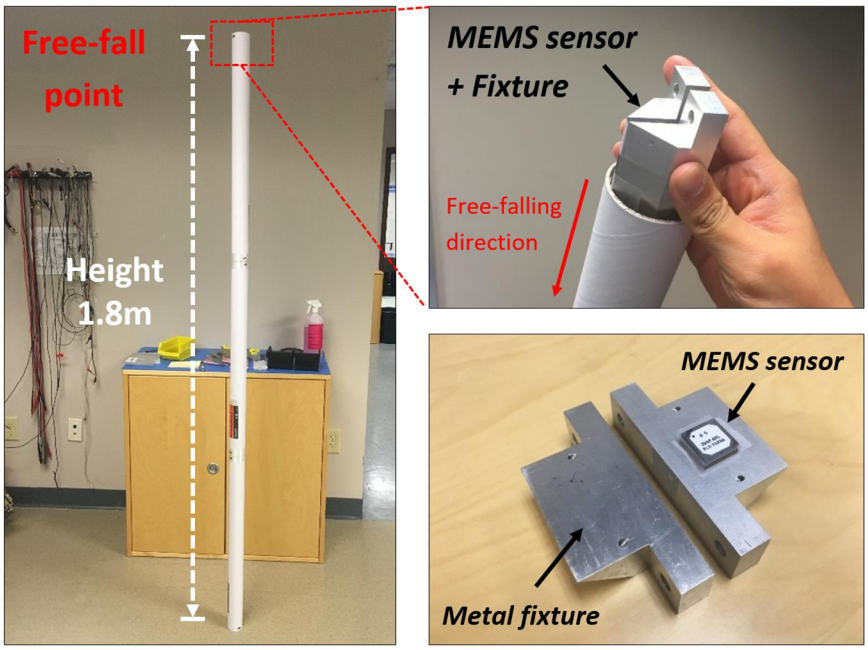


Figure 2. 65: Photograph of free-fall measurement setup to apply high acceleration (>1,000 g) to the MEMS sensor

Such measurement shows that the shock stop, which is enabled using proposed sloped sensing configuration, blocks the excessive proof-mass movement under extreme acceleration condition, and prevents any shock-related damages on the microstructure. Next, the MEMS sensor is undergone through actual acceleration as high as 1,000 g by dropping from the 1.8-meter height (Figure 2. 65). The level of acceleration that is generated by the free-falling impact is calculated using equation (2-23), where v_1 and v_2 represents the velocity of the mass before and after the impact.

$$\vec{a} = \frac{\Delta v}{\Delta t} = \frac{v_1 - v_2}{\Delta t} \qquad (2\text{-}23)$$

The velocity before the impact (v_1) can be calculated using the law of conservation of energy as shown in equation (2-24), where m is the mass, h is height of the free-fall (1.8 meter), and g is the earth gravity (9.8 m/sec^2) respectively.

$$mgh = \frac{1}{2}mv_1^2, \; v_1 = \sqrt{2gh} \qquad (2\text{-}24)$$

The velocity after the impact *(v_2)* is determined by the types of the free-falling collision. If the collision is elastic, v_2 would be same as v_1 with opposite direction *(v_2=-v_1)*, and if the collision is inelastic, v_2 becomes zero *(v_2=0)*. As the metallic mass is dropped toward the hard floor, v_2 is approximated to -0.5·v_1, which is the median value between two collision conditions. From these assumptions, equation (2-25) can be derived.

$$\vec{a} = \frac{v_1 - v_2}{\Delta t} = \frac{1.5\sqrt{2gh}}{\Delta t} \qquad (2\text{-}25)$$

The impact time Δt was chosen to 700 μsec based on the previous study done by the University of Michigan [59], where they reported the impact time Δt ranging from 0.2 to 1.2 msec. From the given values (Δt = 700 μsec and v_2 = -v_1), the acceleration generated by the free-falling can be calculated as 1298 g (=12727.9 m/sec^2). Even at the worst-case scenario (Δt = 1.2 msec and v_2 = 0), the resulting acceleration is 505 g (=4949.75 m/sec^2), which is still far larger than the nominal operational range of proposed design.

The static capacitances (C_P and C_N) of the 12 MEMS devices are measured before and after the free-fall and compared on Figure 2. 66. The average difference *(m)* between two measurements was -5.58 fF, which corresponds to 0.186 % of entire MEMS capacitance (~ 3pF), and the standard deviation *(σ)* was 12.38 fF. Minor differences between each data point are thought to be caused by the measurement error, such as different probe height or equipment settings. It should be noted that none of the MEMS devices showed electrical short even after the free-fall incident. Finally, the MEMS accelerometer was wire-bonded to a switched capacitor ASIC and dropped from a same

1.8-m free-fall setup to validate its effect on the overall performance. Figure 2. 67 compares both sensitivity and offset levels of 4 different devices (MEMS+ASIC) before and after the free-falling. Even after the incident, all the tested devices are still functional and experiences minor variations of 0.78 % on sensitivity and 3 mV on offset level. Considering minor changes on the performance after the free-fall, it can be concluded that high-g shock does not affect the accelerometer operation.

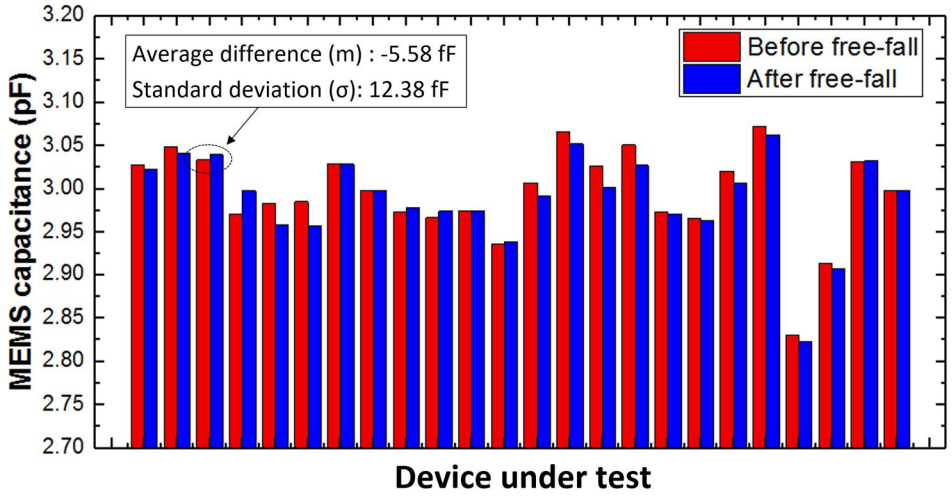


Figure 2. 66: Photograph of free-fall measurement setup to apply high acceleration (>1,000 g) to the MEMS sensor

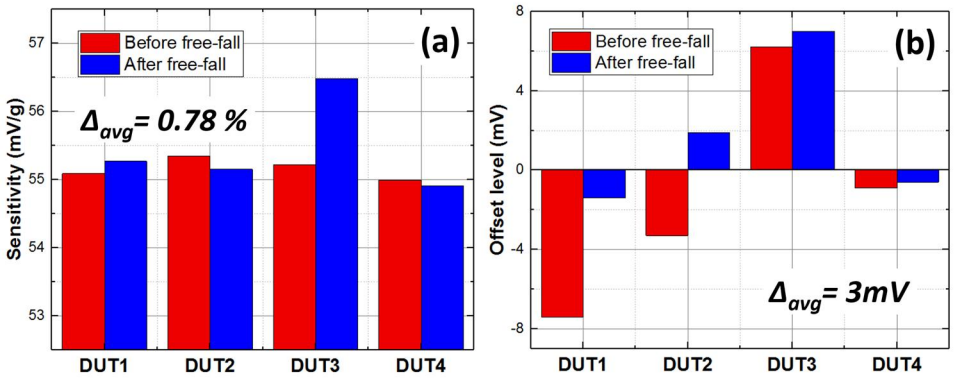


Figure 2. 67: Comparison of measured (a) sensitivity and (b) offset level of MEMS+ASIC before and after the free-fall

Table 2. 6: Performance summary of sloped-electrode in-plane accelerometer

Parameter	Value	Units
Device size	1 × 1 × 0.04	mm^3
Resonant frequency	16.94	kHz
Nano-gap size	270 (Effective sensing gap: 382)	nm
Input acceleration range	± 16	g
Cross-axis sensitivity	0.76 (Y-axis) 1.26 (Z-axis)	%
Noise density level	221 @ 1 Hz	μg/√Hz
Velocity random walk	221.4	μg/√Hz
Bias instability	177.8	μg
Operational bandwidth	> 8.5 (Limited by shaker table)	kHz
BNEA	12.25 (10 Torr)	μg/√Hz

2.6. OUT-OF-PLANE "HINGE-SHAPED" ACCELEROMETER

2.6.1. DESIGN METHODOLOGY

A common method to implement out-of-plane accelerometer is the "teeter-totter" topology [49], in which an imbalance of the proof-mass with respect to the torsional tether creates a torque τ when an external acceleration is applied. This allows the microstructure to rotate at an angle θ, which is expressed by equation (2-18). This equation indicates that the longer the proof-mass length from the torsional support beam *(i.e. r)*, the higher the sensitivity. However, doing so also raises the possibility of stiction due to the capillary force of the wet etchant [44], which is expressed as equation (2-16). During the device release process, liquid etchant (e.g., hydrofluoric acid) that is present at the out-of-plane sensing electrodes would generated a capillary force, which attract the suspended proof-mass toward the fixed microstructure. As the sense electrodes are also located at certain distance from the torsional tether to maximize the capacitive sensitivity, generated torque

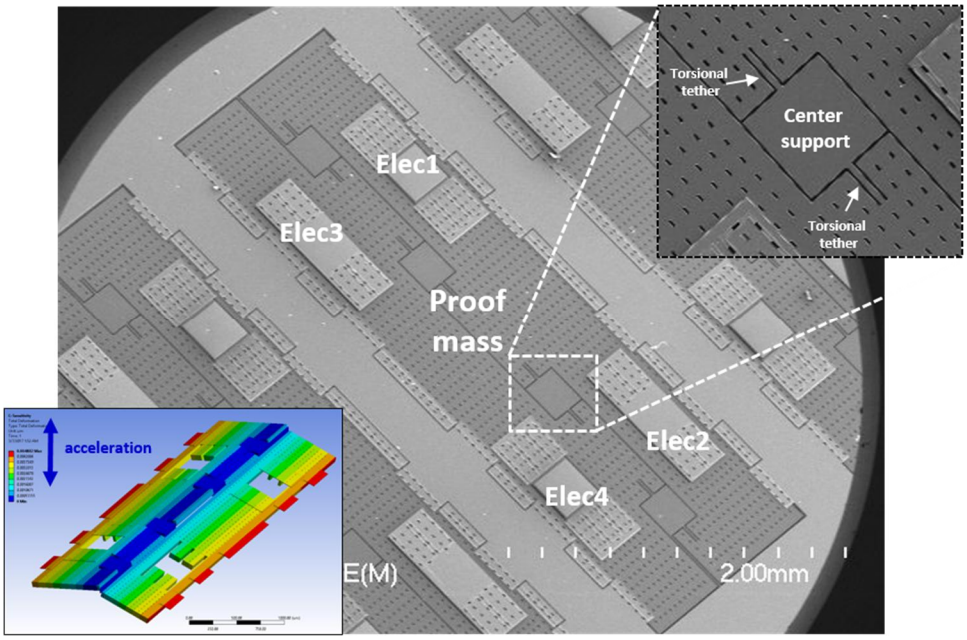


Figure 2. 68: SEM Microphotograph of proposed "hinge-shaped" out-of-plane accelerometer

due to the stiction force would be considerable and can cause a stiction failure if the torque is too excessive. Because of these fabrication-related issues, the proof-mass length from the torsional support beam cannot be increased too much, and thereby limiting the achievable performance using "teeter-totter" topology.

To address such issues, a novel "hinge-shaped" out-of-plane accelerometer is presented [61]. The SEM microphotograph of the fabricated out-of-plane accelerometer is shown on Figure 2. 68 and its movements under external acceleration are depicted in Figure 2. 69. Compared to the conventional torsional design, presented design has a proof-mass width *W* that is larger than its length *L (W>L)*, so that the generated torque due to the capillary force is relatively low. Furthermore, rotational stiffness K_θ of the torsional beam, which is expressed as equation (2-17) was increased by utilizing thick silicon substrate of 60 μm. Figure 2. 68 shows the proof-mass is supported by these eight center-supported

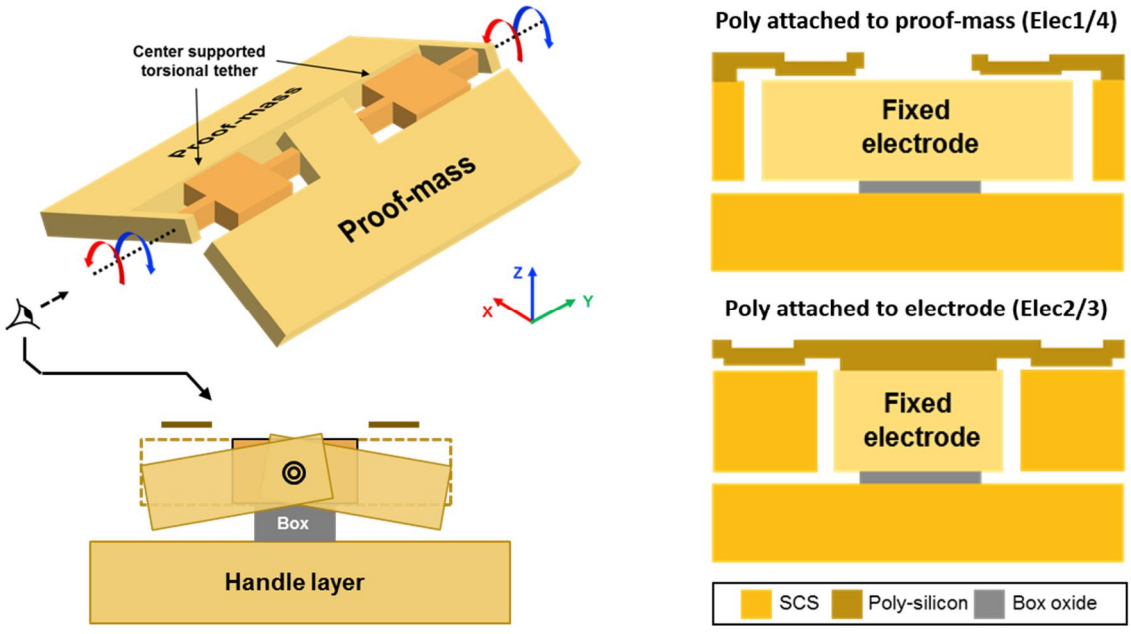


Figure 2. 69: (Left) Simplified schematic diagram of accelerometer movement under acceleration (Right) SEM Microphotograph of proposed "hinge-shaped" out-of-plane accelerometer

torsional tethers, so that the overall rotational stiffness K_θ is increased and the rotated angle due to the capillary force gets reduced, making the device more resilient against stiction.

Such configuration would decrease the capacitive sensitivity, as the generated torque from the acceleration gets reduced. However, this degradation can be compensated by increasing the proof-mass M by utilizing extended width W as well as thicker silicon substrate H_{thk}, following its proportional relationship with the rotated angle θ as expressed in equation (2-18). Furthermore, as the presented design will be utilizing nano-sensing-gap, reduced capacitive sensitivity due to use of stiff structure can be compensated.

The aforementioned design methodology is employed to implement out-of-plane accelerometers with a sensing gap of 300 nm. The proposed accelerometer employs two types of sensing electrodes; one attached to fixed electrode and one attached to movable

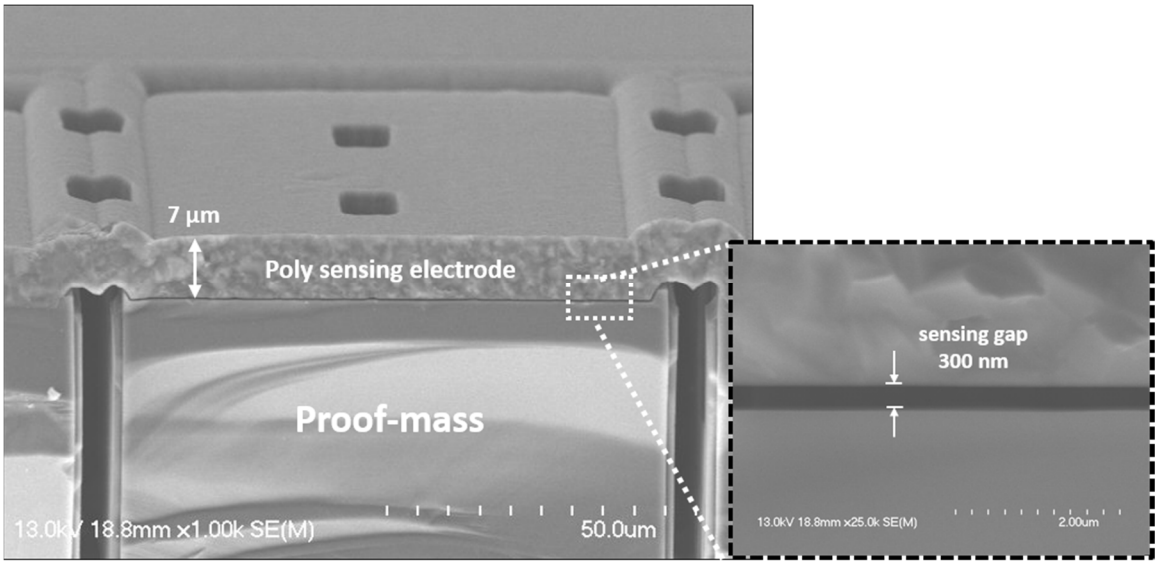


Figure 2. 70: Cross-sectional SEM microphotograph of 300 nm sensing gap between poly-silicon electrode and proof-mass

proof-mass as shown in Figure 2. 69. When the acceleration is applied toward the out-of-plane direction, two gaps increase whereas the other two decrease, creating a differential

capacitance change [43]. A dual proof-mass topology is used to double the capacitive sensitivity. The presented accelerometer is equipped with additional damping electrodes to ensure stable operation under low-pressure environment (~10 Torr).

2.6.2. MEASUREMENT RESULT

Prototypes of the out-of-plane accelerometers are fabricated on a 60 µm thick SOI wafer using HARPSS process [39], where its cross-sectional view is shown on Figure 2. 70. The initial C-V measurements of the fully released devices showed a high fabrication yield (18 out of 23 released devices were functional), validating the efficiency of the "hinge-shaped" design in increasing the device immunity against the stiction during release.

The overall performance of the MEMS accelerometer is characterized by interfacing with the MS3110 Universal Capacitive Readout IC from Irvine Sensors [62] as

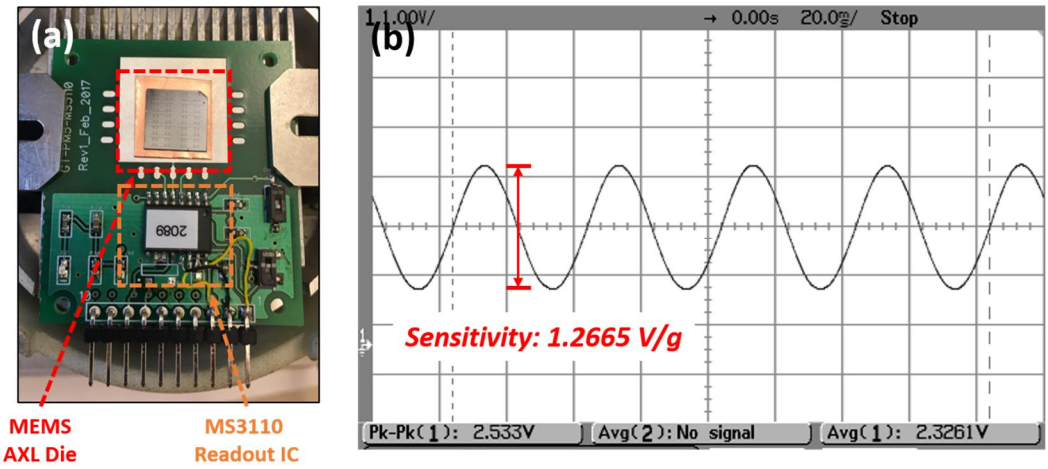


Figure 2. 71: (a) Photograph of evaluation board where MEMS accelerometer is interfaced with MS3110 IC (b) Measured output response under ±1-g 25 Hz sinusoidal acceleration

shown in Figure 2. 71(a). The measured output waveform from Figure 2. 71(b) under ± 1-g sinusoidal acceleration shows that the sensitivity of the proposed device is close to 1266 mV/g. Considering the gain of the circuit is 8.71 mV/g, the capacitive sensitivity of the

device is back-calculated as 145.35 fF/g. To evaluate overall scale-factor of the accelerometer, low0gain setting was used for interface circuit, and higher acceleration levels up to ± 4-g was applied using shaker table. Measured scale factor on Figure 2. 72(a) shows that the cross-axis sensitivity is 2.46 % and 2.89 % for *X*- and *Y*- axis respectively, which is believed to be caused by the poor alignment between the device and the measurement setup as the simulated value was less than 0.1 %.

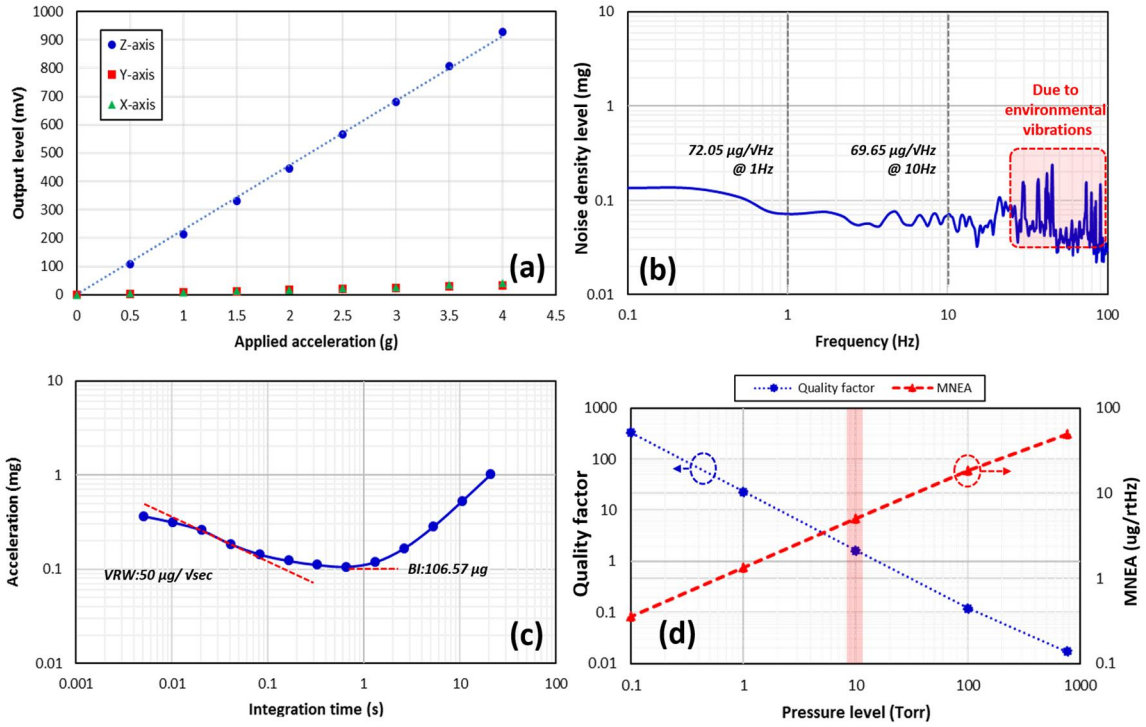


Figure 2. 72: Measured (a) scale factor (b) noise density level and (c) Allan deviation plot of MEMS accelerometer interfaced with ASIC, (d) Simulated quality factor and *BNEA* at different pressure level

The noise performance was evaluated using Agilent 35670A dynamic signal analyzer, and its output spectrum is plotted on Figure 2. 72(b). Measured noise density level is 72.05 µg/√Hz at 1Hz, and 69.65 µg/√Hz at 10 Hz. Finally, the output signal was continuously sampled for a long period to create an Allan Variance plot as shown in Figure 2. 72(c). The bias instability was 106.5 µg and the velocity random walk (VRW) was 50

μg/√Hz. These values are in good agreement with the noise density measurement results presented in Figure 2. 72(b). The fact that the output noise spectrum has higher flicker noise compared to thermal noise indicates that the overall resolution is mostly dominated by the electronics. Additionally, it should be noted that even though the device is designed to be operate at low-pressure level (~10 Torr), it was measured in atmospheric pressure (760 Torr) due to lack of wafer-level vacuum packaging. In atmosphere, the device would be heavily over-damped due to small gaps, which results in increased Brownian noise *(BNEA)* of 48.8 μg/√Hz. This is close to 10 times of increase compared to the estimated BNEA of ~ 5 μg/√Hz at targeted 10 Torr pressure level as shown in Figure 2. 72(d). Figure 2. 72(d) also shows that even though the pressure is reduced to 10 Torr, the operation of accelerometer will be still near critically-damped condition *(Q~0.7)*, resulting in a stable output response. Upon optimization of the readout circuit and by operating the device at moderate vacuum level of ~10 Torr using the wafer capping techniques used in [60], the overall noise performance is expected to reach less than 10 μg/√Hz.

Measured performance summary of hinge-shaped out-of-plane accelerometer is shown on Table 2. 7. Thanks to its revised device geometry compared to conventional torsional accelerometer, the device achieves very high fabrication yield despite having nano-sensing-gaps. Increased electromechanical coupling attained from the nano-gap structure extends the operational bandwidth while attaining μ-g noise level. Lastly, presented design can achieve the stable quasi-static operation in a wide pressure range, yielding a single-digit μ-g noise at 10 Torr pressure.

Table 2. 7: Performance summary of hinge-shaped out-of-plane accelerometer

Parameter	Value	Units
Device size	4 × 1.4 × 0.06	mm^3
Resonant frequency	12.73	kHz
Scale factor	1266 (High-gain) 213 (Low-gain)	mV/g
Device sensitivity	145.35	fF/g
Cross-axis sensitivity	2.46 (X-axis) 2.89 (Y-axis)	%
Noise density level	72.05 @ 1 Hz 69.05 @ 10 Hz	µg/√Hz
Velocity random walk	50	µg/√Hz
Bias instability	106.57	µg
BNEA	2.3 (10 Torr) 34 (1 Torr)	µg/√Hz

2.7. COMPARISON WITH COMMERCIAL ACCELEROMETERS

The measured performance of the presented design is compared with other commercial high-g wide bandwidth accelerometers in Table 3. An appropriate figure-of-merit (FOM) parameter is defined as shown in equation (2-26).

$$FOM = \frac{f_{res}\ [kHz]}{Noise\ density\ [mg/\sqrt{Hz}]} \qquad (2\text{-}26)$$

The comparison table shows that the presented accelerometer has higher figure-of-merit than other commercial counterparts, while providing a much smaller size, meaning that the device can provide low-noise acceleration sensing over a wide range of frequencies. Furthermore, the fact that the nano-gap accelerometer can operate under low-pressure environment without instability issue, becomes a great advantage when implementing

single-chip IMUs using baulk acoustic wave (BAW) gyroscopes. As there is no need for wafer-level-packaging with separate cavity with different pressure, the overall sensor platform can be further miniaturized with reduced fabrication cost.

Table 2. 8: Performance comparison with commercial wide-bandwidth accelerometers

Parameter	Noise density level (mg/√Hz)	F_{res} (kHz)	FOM
ADXL001 [37]	3.3	22	6.67
ADIS6228	0.248	5.5	22.17
MMA685X	1.25	13.33	10.664
KX222-1054 [36]	0.76 (in-plane) 1.2 (out-of-plane)	6 (in-plane) 3.6 (out-of-plane)	7.89 (in-plane) 3 (out-of-plane)
Sloped-electrode IPA	**0.221**	**16.94**	**76.65**
Hinge-shaped OPA	**0.05**	**12.7**	**254**

3. MEMS ACCELEROMETER SIGNAL CONDITIONING INTEGRATED CIRCUIT

In this chapter, design and characterization of interface circuit, which converts the capacitance change of the MEMS accelerometer into an electrical signal, will be discussed in detail. The entire section starts by introducing existing readout topologies for MEMS accelerometer, comparing pros and cons between each configuration, and move on to the actual circuit implementation as well as characterization. Because the MEMS accelerometer has relatively low operational bandwidth (DC ~ 1 kHz) compared to other existing applications, the entire circuit may suffer from large 1/f noise or DC offset from the amplifier if proper noise reduction method is not used. To address such issues, number of different dynamic noise reduction techniques [63], such as chopper stabilization or correlated-double-sampling (CDS) are employed. Furthermore, due to the mode of operation, any capacitance mismatch on the MEMS sensor can create a large offset that directly impacts on the system dynamic range. To address such issues, a novel calibration method is proposed and various measurements were done to validate its effectiveness.

3.1. CT VS DT READOUT SCHEME

Depending on the modes of operation, the readout topologies for accelerometer interface circuit are divided into two categories; continuous-time (CT) [64] and discrete-time sensing (DT) [65]-[66]. The schematic diagram of CT sensing circuit is shown on Figure 3. 1, which is consisted of transimpedance amplifier (TIA), down-conversion mixer and low-pass filter (LPF). The capacitor C_P and C_N represent the changing capacitances of the MEMS accelerometer, which common node A (substrate) is tied to the input of TIA.

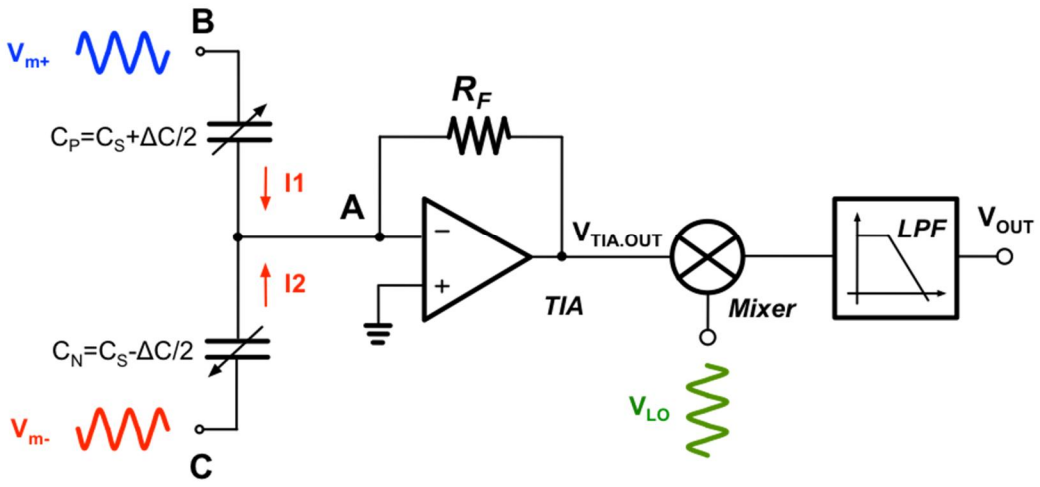


Figure 3. 1: Schematic diagram of CT (continuous-time) accelerometer sensing circuit

During operation, the other two terminals *B* and *C* (sensing electrodes) are excited with different modulation voltages ($=Asin(\omega_m t)$) with opposite phase, so that the differential currents I_1 and I_2 are generated from the MEMS capacitor as expressed in equation (3-1).

$$I_1 = C_P \cdot A\omega_m \cos(\omega_m t), \quad I_2 = -C_N \cdot A\omega_m \cos(\omega_m t) \qquad (3\text{-}1)$$

These currents are merged at node *A*, and its difference $(I_1\text{-}I_2)$ is amplified by the TIA gain *R* as expressed in equation (3-2). As this output still contains high frequency carrier signal (ω_m), down-conversion mixer is added to demodulate the acceleration signal into the baseband as shown on equation (3-3). The upconverted high frequency carrier signal ($2\omega_m$) is removed using low-pass-filter (LPF) as equation (3-4).

$$V_{TIA.OUT} = -R \cdot (I_1 + I_2) = -(C_P - C_N) \cdot R \cdot A\omega_m \cos(\omega_m t) \qquad (3\text{-}2)$$

$$V_{mixer} = -\Delta C \cdot R \cdot A\omega_m \cos(\omega_m t) \times A\cos(\omega_m t) = -\frac{1}{2} A^2 R\omega_m \cdot \Delta C \cdot [1 + \cos(2\omega_m t)] \quad (3\text{-}3)$$

$$V_{LPF.OUT} = -\frac{1}{2} A^2 R\omega_m \cdot \Delta C \qquad (3\text{-}4)$$

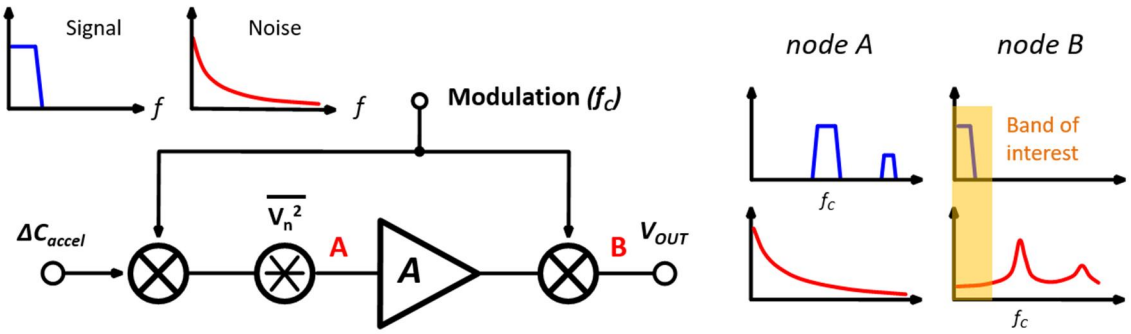


Figure 3. 2: Concept diagram of chopper stabilization used in accelerometer interface circuit

The use of modulation scheme helps to achieve improved signal-to-noise ratio by upconverting amplifier noise (i.e., Chopper stabilization [63]) as shown on Figure 3. 2. Whereas the acceleration signal is modulated and then demodulated back to baseband, the noise of the amplifier ($\overline{V_n^2}$) is modulated only once, and stays at high frequency region. It can be seen from the Figure 3. 2 that within the operational bandwidth of interest, the node *B* has far better signal-to-noise ratio compared to node *A*. CT sensing circuit has advantage that the capacitance change can be converted into the voltage with precision noise performance using relatively simple architecture compared to DT sensing configuration. However, to account for the high frequency modulation signal, the amplifier needs to have wide operational bandwidth, which results in large power consumption. In addition, to meet the low cut-off frequency requirement of the LPF block, the circuit requires large passive components (R and C), which makes the CT sensing circuit suitable for printed-circuit-board (PCB) implementation rather than integrated-solution.

DT sensing topology, which schematic is shown Figure 3. 3, uses switched-capacitor (SC) circuit to consecutively charge and discharge the MEMS accelerometer and convert capacitance change into the voltage. To suppress large DC offset and 1/f noise of the amplifier, CDS technique or chopper stabilization method [63] is often incorporated

into the design. The DT sensing circuit is popular to most of the commercial accelerometers [20]-[24], for its lower power consumption compared to that of CT sensing approach. Furthermore, the topology is more suitable for integrated IC as it does not require large low-pass filter, and can be easily interfaced with ΣΔ ADC, which also operates in discrete-time domain. As we will be focusing more on the integrated solution, DT sensing topology is chosen to convert the movement of the MEMS accelerometer into an electrical signal, and its detailed operation is explained on following section.

3.2 Interface Circuit Design

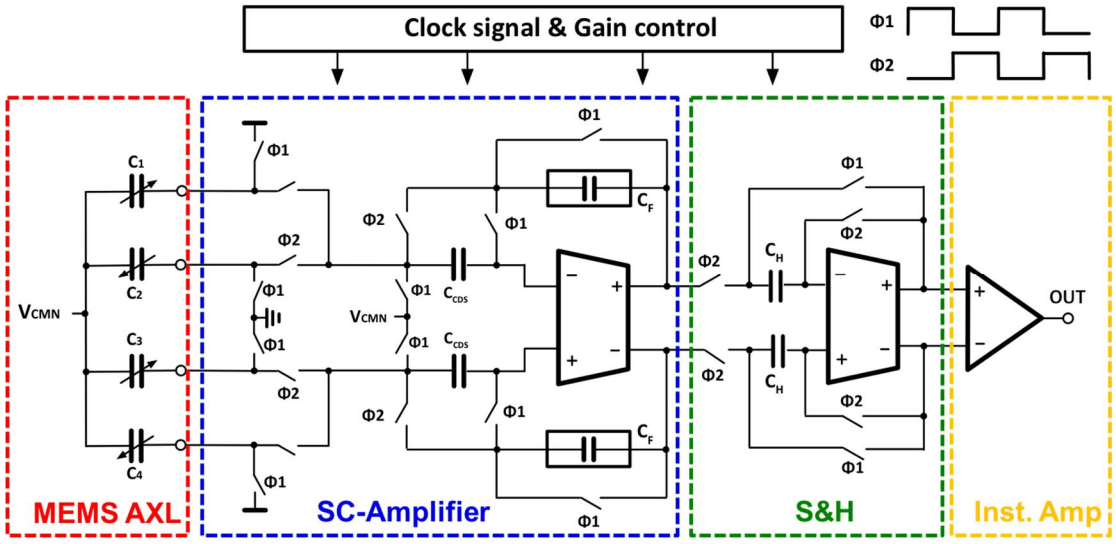


Figure 3. 3: Schematic diagram of proposed readout circuit for MEMS accelerometer

Figure 3. 3 shows the overall schematic diagram of the proposed interface circuit, which is consisted of SC-amplifier, S&H block, and instrumentation amplifier that is used to convert differential signal into a single-ended output. The entire circuit is controlled by a non-overlapped clock-signals that are generated internally. Based on the measurement results of the fabricated MEMS accelerometer from prior section, required specification table for the interface circuit is summarized as Table 3. 1.

Table 3. 1: Required specification for interface circuit for MEMS accelerometer

Specification parameter	Value
Clock frequency (f_{CLK})	≥ 100 kHz
Linearity error	≤ 0.1 %
Supply voltage (VDD)	3 V
Static capacitance (C_S)	4 pF per each electrode
Capacitance to voltage gain (CV_{gain})	≥ 15 mV/fF
Feedback capacitance (C_F)	≤ 100 fF

3.2.1. SC AMPLIFIER DESIGN

The operation of DT sensing circuit is controlled by the two non-overlapping clock phases as shown in Figure 3. 4 and Figure 3. 5 [67]. During charging phase ($\Phi_1=1, \Phi_2=0$), each sense electrode *($C_1/C_2/C_3/C_4$)* of the accelerometer is connected to either the supply *(VDD)* or the ground *(VSS)* depending on the connection. As the other terminal of the MEMS accelerometer (i.e. substrate) is tied to the V_{CMN} *(=0.5VDD)*, there would be *0.5VDD* voltage difference across the MEMS capacitor, which would store charges that are equivalent to equation (3-5) to (3-8).

Both operational-transconductance-amplifier (OTA) and S&H block is connected in unity-gain configuration at this phase ($\Phi_1=1, \Phi_2=0$). The input of OTA is tied to CDS capacitor to store 1/f noise and DC offset, which is denoted as V_{OS} in Figure 3. 4.

$$Q_1 = (VDD - V_{CMN}) \cdot C_1 = 0.5 \cdot VDD \cdot (C_s + \Delta C_{accel}/4) \quad (3\text{-}5)$$

$$Q_2 = (VSS - V_{CMN}) \cdot C_2 = -0.5 \cdot VDD \cdot (C_s - \Delta C_{accel}/4) \quad (3\text{-}6)$$

$$Q_3 = (VSS - V_{CMN}) \cdot C_3 = -0.5 \cdot VDD \cdot (C_s + \Delta C_{accel}/4) \quad (3\text{-}7)$$

$$Q_4 = (VDD - V_{CMN}) \cdot C_3 = 0.5 \cdot VDD \cdot (C_s - \Delta C_{accel}/4) \quad (3\text{-}8)$$

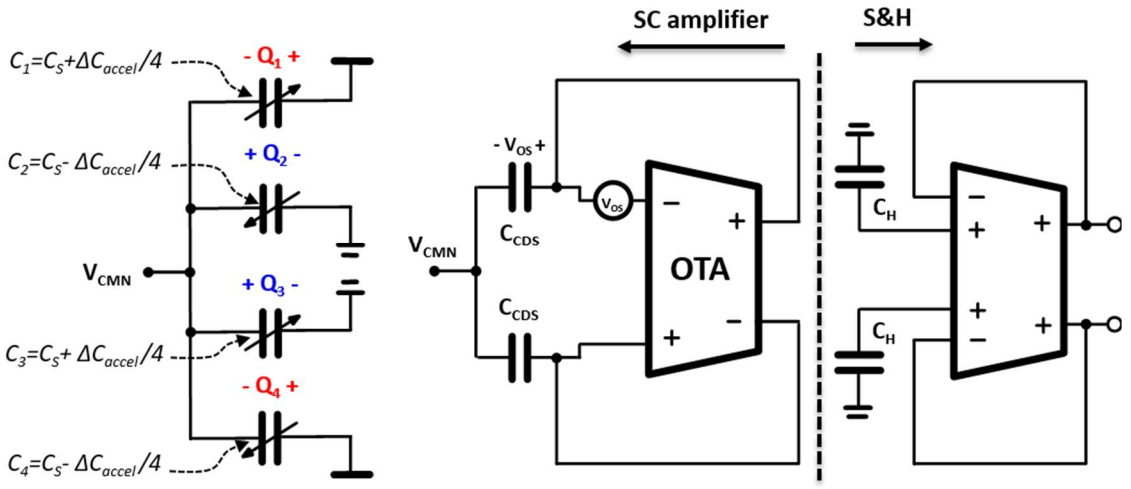


Figure 3. 4: SC amplifier and S&H block configuration during charging phase ($\Phi_1=1, \Phi_2=0$)

During amplification phase ($\Phi_1=0, \Phi_2=1$), the switch connection is changed so that charged MEMS capacitors, C_1/C_2 and $C_3/C4$ are tied to each other at summing node V_{i-} and V_{i+} along with feedback capacitor C_F as shown in Figure 3. 5. Based on the law of charge conservation, the charges at the amplification phase is equivalent to the stored charges at the charging phase that are shown on equation (3-5) to (3-8). From this relationship, equation (3-9) can be derived as below.

$$\begin{cases} 0.5VDD\cdot(C_1-C_2)=(C_1+C_2)\cdot(V_{i-}-V_{CMN})+C_F\cdot(V_{i-}-V_{OUT+}) \\ 0.5VDD\cdot(-C_3+C_4)=(C_3+C_4)\cdot(V_{i+}-V_{CMN})+C_F\cdot(V_{i+}-V_{OUT-}) \end{cases} \quad (3\text{-}9)$$

Both V_{i-} and Vi+ can be expressed as equation (3-10) using the superposition between common-mode (V_{CMN}) and differential voltage.

$$V_{i+}=V_{CMN}+\frac{v_{id}}{2},\ V_{i-}=V_{CMN}-\frac{v_{id}}{2} \quad (3\text{-}10)$$

Using the property of the ideal op-amp, the differential output can be expressed as equation (3-11) and used to derive equation (3-12). A_{OL} denotes open-loop-gain of OTA.

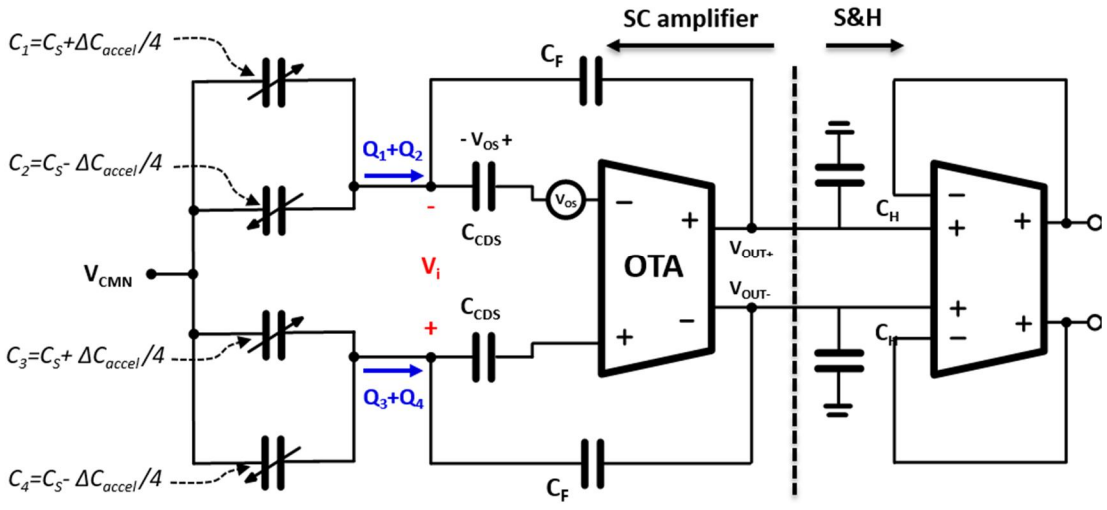


Figure 3. 5: SC amplifier and S&H block configuration during amplification phase ($\Phi_1=0$, $\Phi_2=1$)

$$\Delta V_{OUT} = A_{OL}(V_{i+} - V_{i-}) \Rightarrow V_{OUT+} = V_{CMN} + A_{OL}\frac{v_{id}}{2}, V_{OUT-} = V_{CMN} - A_{OL}\frac{v_{id}}{2} \qquad (3\text{-}11)$$

$$V_{i+} = V_{CMN} + \left(\frac{V_{CMN} - V_{OUT-}}{A_{OL}}\right), V_{i-} = V_{CMN} + \left(\frac{V_{CMN} - V_{OUT-}}{A_{OL}}\right) \qquad (3\text{-}12)$$

By replacing V_{i-} and V_{i+} at equation (3-9) with (3-12), equation (3-13) is derived.

$$\begin{cases} 0.5VDD \cdot \dfrac{\Delta C_{accel}}{2} = (2C_S + C_F)\cdot\left(V_{CMN} + \dfrac{V_{CMN} - V_{OUT-}}{A_0}\right) - 2C_S \cdot V_{CMN} - C_F \cdot V_{OUT+} \\ -0.5VDD \cdot \dfrac{\Delta C_{accel}}{2} = (2C_S + C_F)\cdot\left(V_{CMN} + \dfrac{V_{CMN} - V_{OUT+}}{A_0}\right) - 2C_S \cdot V_{CMN} - C_F \cdot V_{OUT-} \end{cases} \qquad (3\text{-}13)$$

This equation can be further simplified using number of properties. As the open-loop gain *(A_{OL})* of the OTA is high, both $(V_{CMN} - V_{OUT-})/A_{OL}$ and $(V_{CMN} - V_{OUT+})/A_{OL}$ can be neglected. Also, $2C_S+C_F$ can be approximated to $2C_S$ as MEMS capacitor is orders of higher than feedback capacitor C_F. Based on this relationship, equation (3-13) is further

simplified as equation (3-14), and by subtracting these two equations, the overall transfer function of the SC-amplifier can be derived as equation (3-15).

$$0.5VDD \cdot \frac{\Delta C_{accel}}{2} = -C_F \cdot V_{OUT+}, \quad -0.5VDD \cdot \frac{\Delta C_{accel}}{2} = -C_F \cdot V_{OUT-} \qquad (3\text{-}14)$$

$$\therefore \Delta V_{OUT} = V_{OUT+} - V_{OUT-} = -\frac{0.5VDD}{C_F} \Delta C_{accel} \qquad (3\text{-}15)$$

During amplification phase ($\Phi_1=0,\ \Phi_2=1$), the CDS capacitor connection is changed so that the stored DC offset and 1/f noise, which is denoted as V_{OS}, has opposite polarity with that of the OTA (Figure 3. 5). At this configuration, the CDS capacitor behaves as a battery with inverted polarity -V_{OS} that cancels out the OTA noise V_{OS} on the amplification path. In the meantime, S&H block [68] holds the SC-amplifier output to C_H to convert discrete-time signal into the continuous-time output.

The switches inside the SC-amplifier are implemented using MOSFET transistor. To minimize the on-state resistance (R_{ON}), both PMOS and NMOS transistors are used to create transmission gate switch. The sizes of the different types of transistors were adjusted to reflect the difference on the mobility between PMOS and NMOS transistors. Although there are several non-ideal effects such as charge-injection [69] or clock feedthrough [70] that alters the performance of SC interface, use of fully-differential topology would mitigate such effect by treating them as common-mode variation.

3.2.2. SUB-CIRCUIT BLOCK DESIGN

The required open-loop DC gain (A_{OL}) and unify gain bandwidth ($f_{\_0dB}$) of the OTA is chosen based on the capacitive feedback network of the SC-amplifier at amplification

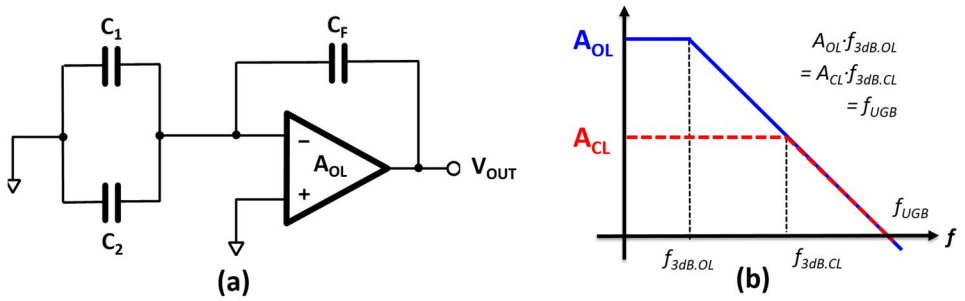


Figure 3. 6: (a) Capacitive feedback configuration of SC amplifier during amplification phase (b) Comparison between open-loop and closed-loop frequency response

phase (Φ_1=0, Φ_2=1), which is shown on Figure 3. 6(a). For simplicity, only half-circuit schematic is depicted. Closed-loop gain (A_{CL}), feedback ratio (β), and the loop-gain (L) are expressed in equation (3-16) to (3-18).

$$A_{CL} = \frac{A_{OL}}{1 + A_{OL}\beta} \qquad (3\text{-}16)$$

$$\beta = \frac{Z_{C_1} \| Z_{C_2}}{Z_{C_F} + (Z_{C_1} \| Z_{C_2})} \approx \frac{C_F}{C_1 + C_2} \qquad (3\text{-}17)$$

$$Loop\ gain\ (L) = A_{OL} \times \beta \qquad (3\text{-}18)$$

As the static capacitances C_1 and C_2 are 4 pF per electrode, and the feedback capacitance C_F at maximum gain setting is 100 fF (CV_{gain}=15 mV/fF), the feedback factor (β) of the SC-amplifier becomes 0.0125 (=-38.06 dB). The required loop-gain (L) is calculated as 60 dB based on the non-linearity requirement of 0.1 % using the equation (3-19) [71]. To compensate for extremely low feedback factor (β) and maintain sufficient loop-gain (L), the open-loop gain of the amplifier (A_{OL}) needs to be higher than 98.06 dB.

$$Linearity\ Error = \frac{1}{1+L} = \frac{1}{1 + A_{OL}\beta}\ [\%] \qquad (3\text{-}19)$$

Required unity gain bandwidth *(f_{UGB})* of the OTA is calculated by using equation (3-20), where the closed loop 3-dB bandwidth is assumed as target clock frequency *($f_{3dB.CL}$=100 kHz)* from Table 3. 1. The calculation shows the OTA need to have unity gain bandwidth *(f_{0dB})* larger than 8 MHz.

$$f_{UGB} = A_{CL} \times f_{3dB.OL} = A_{CL} \times f_{3dB.CL} \approx \frac{1}{\beta} \times f_{3dB.CL} \qquad (3\text{-}20)$$

To satisfy high DC gain (>98.06 dB) and wide bandwidth (> 8MHz), folded-cascode fully differential amplifier with gain-boosted technique[72] is chosen as OTA topology, which schematic is shown in Figure 3. 7.

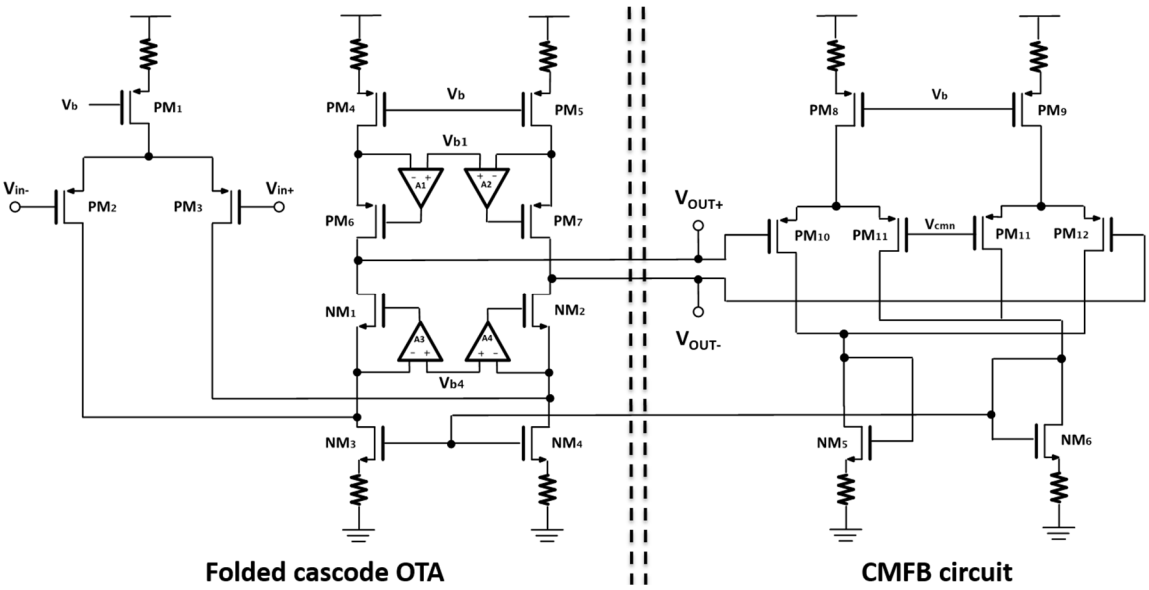


Figure 3. 7: Schematic of gain-boosted fully-differential folded-cascode OTA with CMFB circuit

Increased output resistance attained by cascode transistor connected in gain-boosted configuration [72] enables achieving far increased DC gain than any other amplifier configurations. Negative feedbacks formed with error amplifiers *A1~A4* increase the output resistance by its gain A_{err}. Also, the source nodes of the transistors *NM1, NM2,*

PM6, & PM7 are set close to the bias voltage V_{b1} and V_{b2}, so that transistor operation is forced to saturation region. The overall gain of the OTA is expressed as equation (3-21).

$$A_{OL} = G_m R_{out} = g_{m2} \cdot (A_{err} \cdot g_{m2} r_{ds2} (r_{ds4} \,||\, r_{ds3}) \,||\, A_{err} \cdot g_{m7} r_{ds7} r_{ds5}) \qquad (3\text{-}21)$$

As folded-cascode OTA has high output resistance at the differential pair, any current mismatch caused by process or temperature variation may create a large DC offset, and can rail the output. To address such issues, common-mode-feedback (CMFB) network circuit using differential-difference amplifier (DDA) [74] is added to detect perturbation on output common-mode voltage *(=(V_{OUT+}+V_{OUT-})/2)* and generate a control signal to null out the unwanted offset [73]-[74]. If the common-mode voltage increases, the current flowing on input CMFB transistors *PM10* and *PM13* decreases due to lesser gate-source voltage *(V_{GS})*. On the other hand, the other transistor *PM11* and *PM12,* which is biased with the constant reference voltage *(=V_{CMN})*, would induce more currents from the constant current sources *PM8* and *PM9*. Such change creates a voltage difference between two diode-connected transistors *NM5* and *NM6,* and increases the control signal (i.e., gate-source voltage on transistor *NM3* and *NM4*) of the folded-cascode amplifier. Increased current at the output pair pulls down the common-mode voltage on the output to the reference level. If the common-mode voltage decreases, the CMFB circuit will generate control signal with opposite behavior.

The noise model of the fully-differential folded-cascode amplifier is shown at Figure 3. 8. For simplicity, only the half circuit is shown and the PMOS current sourcing transistors are replaced with ideal components, I_{B1} and I_{B2}. The output noise $\overline{V_{n.out}}^2$ is

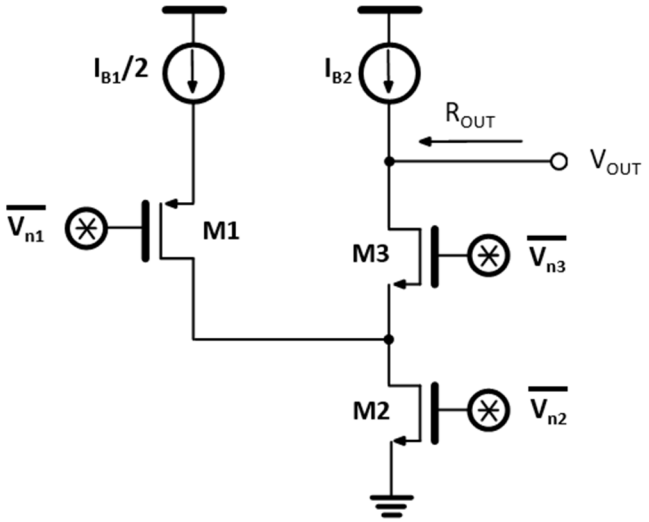


Figure 3. 8: Noise model of fully-differential folded-cascode amplifier (Half circuit)

expressed as equation (3-22). By dividing the output noise with the gain of the amplifier is $g_{m1}R_{OUT}$, the input referred noise $\overline{V_{n.in}}^2$ is derived as equation (3-23).

$$\overline{V_{n.out}}^2 = (g_{m1}R_{OUT})^2 \cdot \overline{V_{n1}}^2 + (g_{m2}R_{OUT})^2 \cdot \overline{V_{n2}}^2 + \overline{V_{n3}}^2 \qquad (3\text{-}22)$$

$$\overline{V_{n.in}}^2 = \overline{V_{n1}}^2 + \left(\frac{g_{m2}}{g_{m1}}\right)^2 \cdot \overline{V_{n2}}^2 + \left(\frac{1}{g_{m1} \cdot R_{OUT}}\right)^2 \cdot \overline{V_{n3}}^2 \qquad (3\text{-}23)$$

From the analysis, it is concluded that input transistor M_1 is the major noise source of the folded-cascode amplifier. Therefore, the size of the input transistor needs to be large enough to suppress 1/f noise, and to increase g_m for less thermal noise. Furthermore, as mentioned earlier, dynamic noise reduction techniques, such as chopper-stabilization and CDS are required in SC-amplifier to suppress the noise of the OTA.

It is also noted from equation (3-24) that current-sourcing transistor M_2 is the 2nd major noise source of the entire amplifier. Although it is possible to reduce the noise by increasing transistor size, doing so has limitation that it can alter the biasing condition of

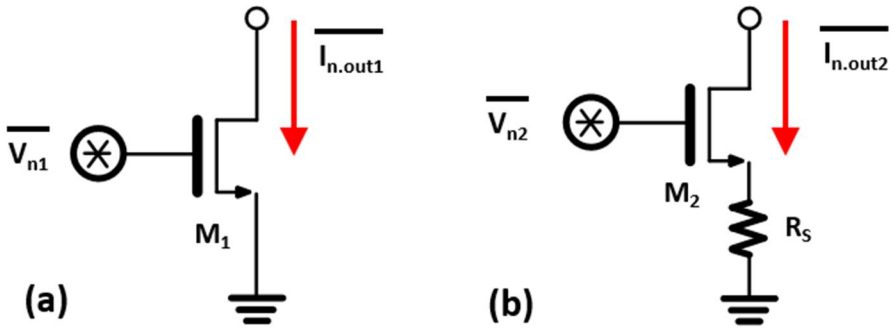


Figure 3. 9: Comparison of noise model between transistor (a) without and (b) with source-degeneration

the current-sourcing transistors. As an alternative, source-degeneration technique [75] is introduced to lower the noise in current-sourcing transistor. Figure 3. 9 shows the comparison of transistor noise model with and without source degeneration.

As can be seen from the noise current expression on equation (3-24) and (3-25), by degenerating its source, the transistor noise is reduced by the factor of $1+g_mR_S$. In ordinary case, source-degeneration noise reduction method is not recommended as it also lowers the entire amplifier gain and does not affect the input-referred noise. However, for current-sourcing transistor, which transconductance (g_m) is independent of the amplifier gain, source-degeneration can be a simple but effective way to lower the 1/f noise.

$$\overline{i_{n.out1}}^2 = g_{m1}{}^2 \cdot \overline{v_n}^2 \qquad (3\text{-}24)$$

$$\overline{i_{n.out2}}^2 = G_{m2}{}^2 \cdot \overline{v_n}^2 = \left(\frac{g_{m2}}{1+g_{m2}R_S}\right)^2 \cdot \overline{v_n}^2 \qquad (3\text{-}25)$$

Performance of the OTA was verified using Cadence Spectre and its results are plotted on Figure 3. 10. Simulated DC gain is 114.4 dB, phase margin was 87.97 º, and the unity gain bandwidth was 8.4 MHz, which satisfies the target specification in Table 3. 1.

Designed OTA was used to implement SC-amplifier, which schematic is shown on Figure 3. 3, and both transient and PNOISE simulations were conducted as shown in Figure 3. 11. While running transient simulation, changing capacitance of MEMS accelerometer was modeled as time-varying capacitor using VerilogA. Furthermore, CDS function was intentionally disabled to compare the noise performance with the case when the CDS is enabled, showing more than 5 times of noise reduction (Figure 3. 11(b)).

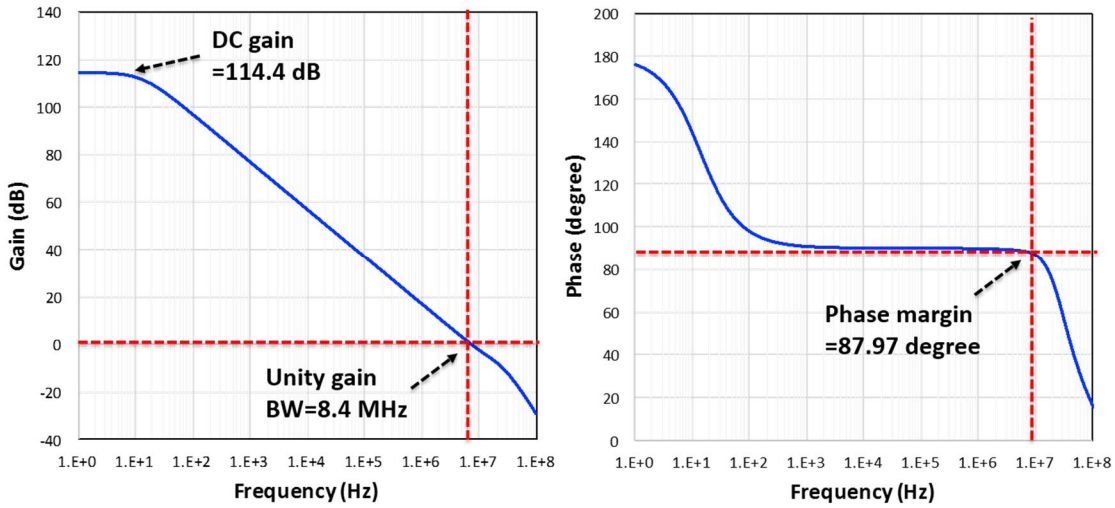


Figure 3. 10: Simulated frequency response of the fully-differential OTA

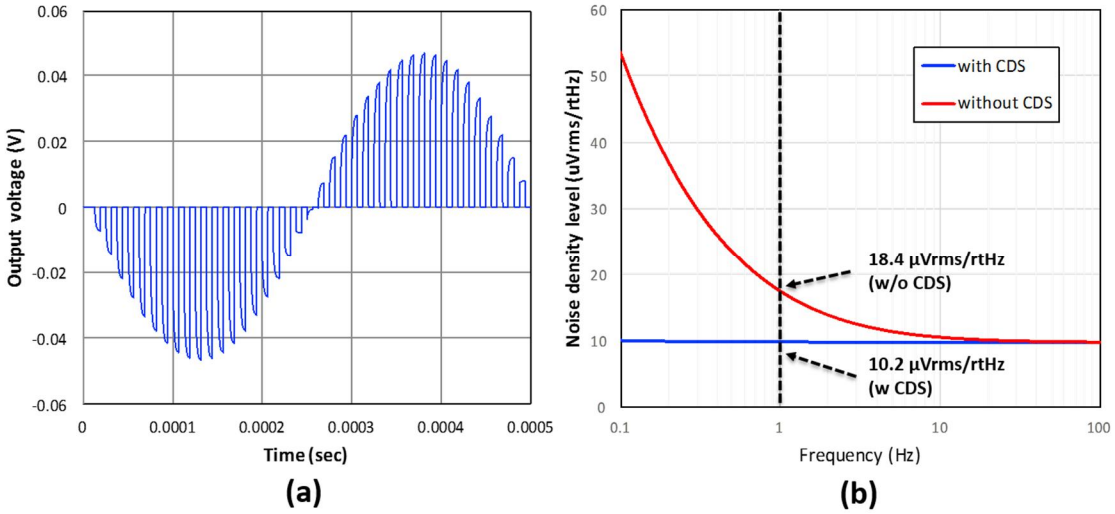


Figure 3. 11: (a) Transient simulation result of SC-amplifier under sinusoidal capacitance change (b) PNOISE simulation result when CDS operation was enabled and disabled

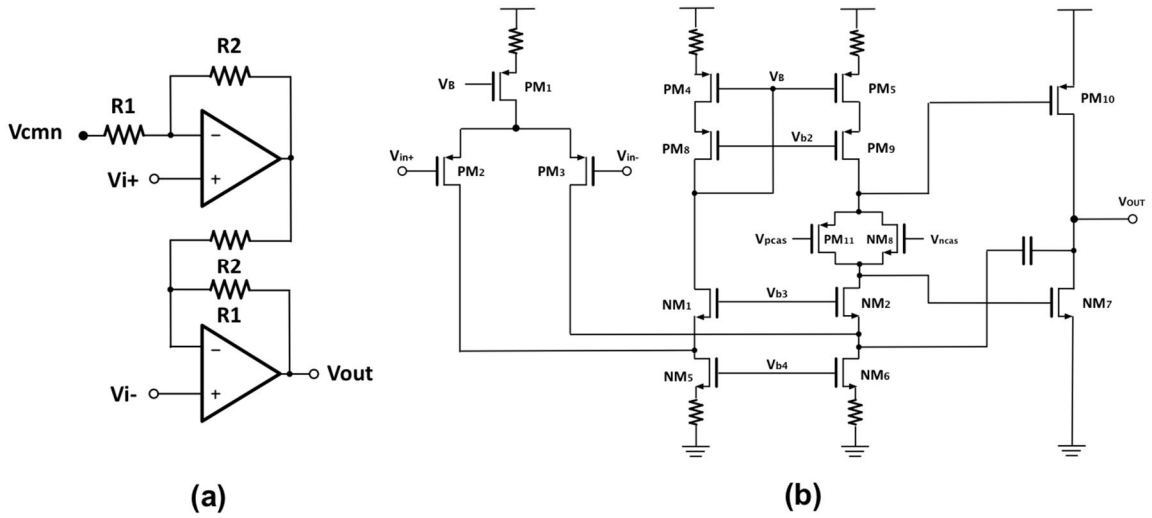


Figure 3. 12: (a) Schematic of instrumentation amplifier and (b) Folded-cascode amplifier with class-AB output stage

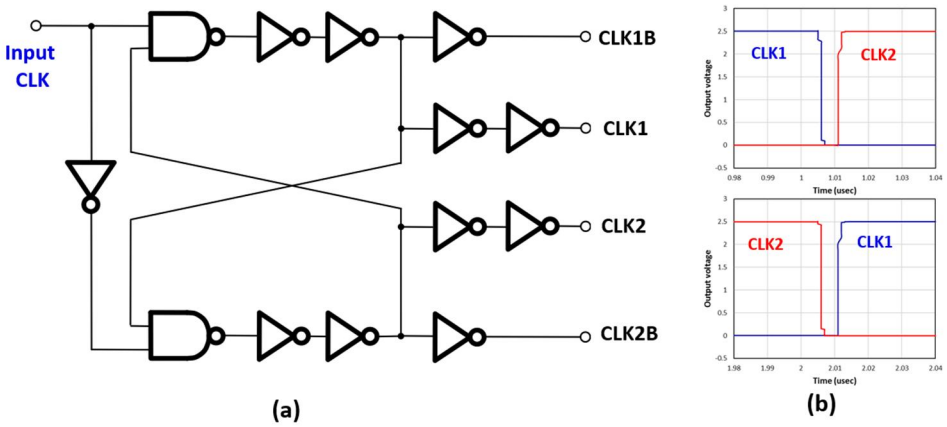


Figure 3. 13: (a) Schematic of non-overlapping clock generation block and (b) transient simulation result between each clock phase at rising and falling edge

The differential output from the S&H block is converted to single-ended output using instrumentation amplifier, which schematic is shown on Figure 3. 12(a). The block is consisted of two differential amplifiers connected in inverted configuration with resistors R_1 and R_2. The transfer function of the instrumentation amplifier is expressed as equation (3-26). The differential amplifier itself is a folded-cascode amplifier with class-AB stage[68],[72] as shown on Figure 3. 12(b).

$$V_{OUT} = \left(1 + \frac{R_1}{R_2}\right) \cdot (V_+ - V_-) \qquad (3\text{-}26)$$

The non-overlapping clock signals for controlling switched capacitor interface circuits, are generated using cross-coupled inverter chains as shown on Figure 3. 13(a). Simulation result on Figure 3. 13(b) shows non-overlapping period between each clock phase is around 3 to 4 nsec.

3.2.3. SIMULATION AND MEASUREMENT RESULT

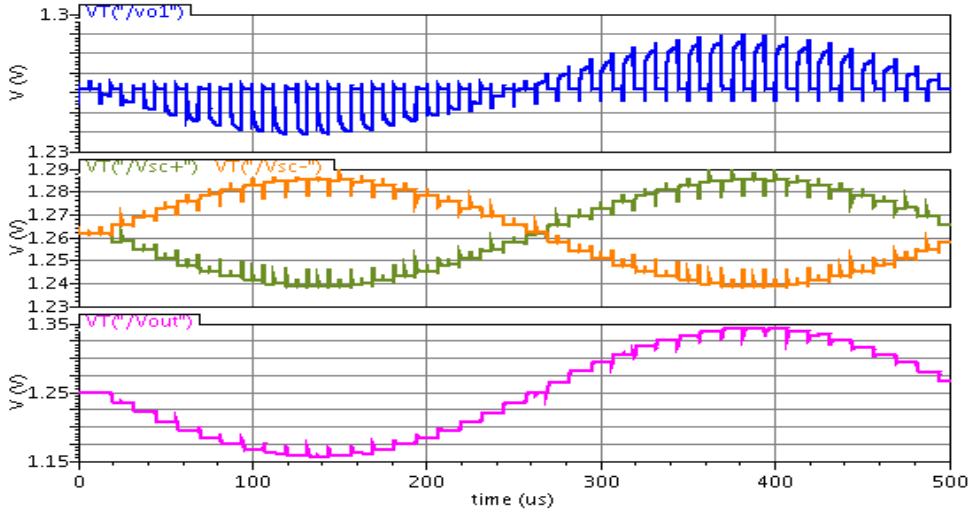


Figure 3. 14: Simulated transient response from the accelerometer interface circuit

Transient simulation on entire interface circuit was conducted to fully validate its functionality, where Figure 3. 14 shows the outputs of each sub-block (SC-amplifier, S&H, and Instrumentation amplifier) when the MEMS capacitances experience a sinusoidal variation. Number of glitches were observed at the output of the S&H block due to charge-injections and clock feedthrough [69][70]. However, thanks to using fully-differential topology, it is observed that such non-ideal behaviors are suppressed at the final output. Figure 3. 15(a) shows the output level of the interface circuit with respect to capacitance

change to calculate the capacitance-to-voltage gain of the circuit, which is 60mV/fF at maximum gain setting. PNOISE simulation result at Figure 3. 15(b) shows simulated input referred noise density level is 181 µg/rtHz at 1 Hz frequency.

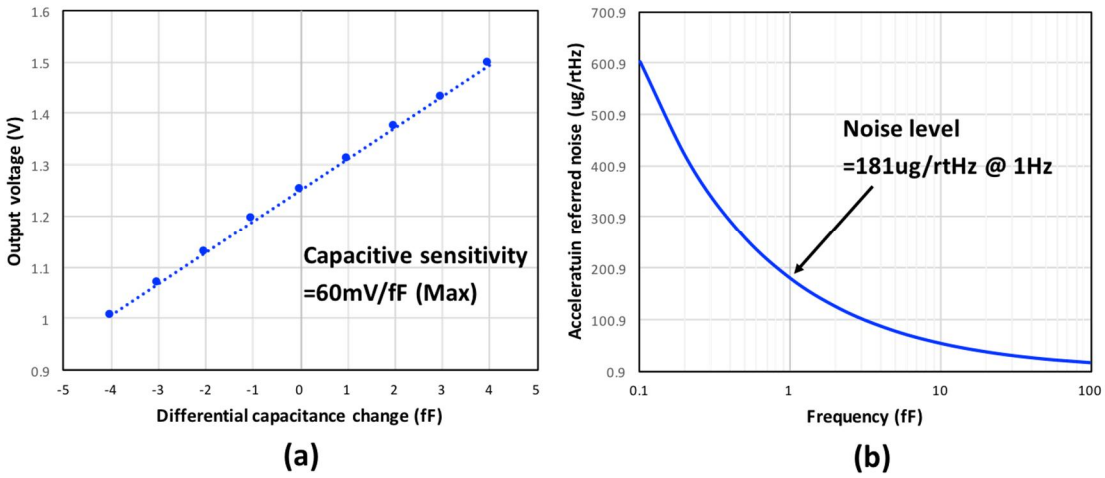


Figure 3. 15: Simulated (a) capacitance to voltage gain under maximum setting and (b) PNOISE simulation result of the interface accelerometer circuit

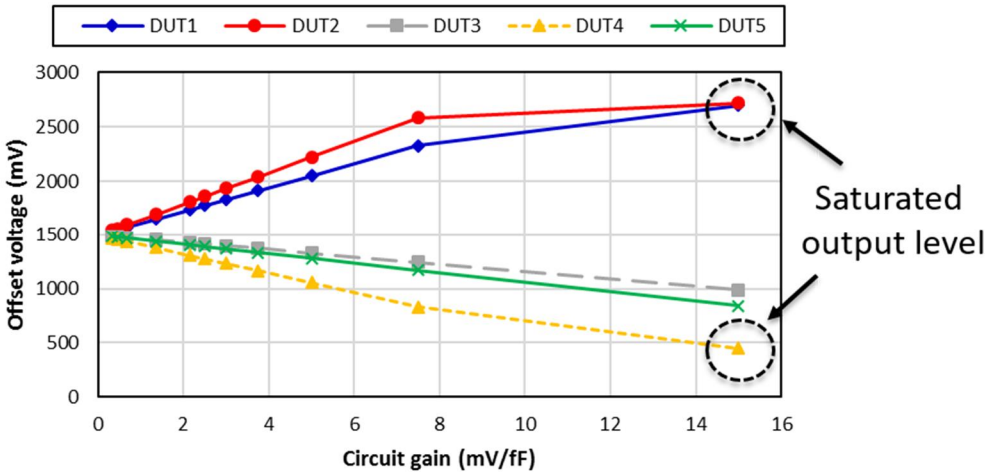


Figure 3. 16: Measured output level with respect to gain of the interface circuit

Presented interface circuit is fabricated using TSMC 0.18 µm 2P6M CMOS process and wire-bonded to the wafer-level packaged MEMS accelerometer *(Gen-1 design)* as shown in Figure 2. 32. Other measurement results such as output waveform (Figure 2. 33), scale-factor (Figure 2. 34), and noise density measurements (Figure 2. 35) are already

shown in Chapter 2. During characterization process, it is observed that the output has an offset that changes with respect to capacitance-to-voltage gain of the circuit as shown in Figure 3. 16. If the circuit gain setting is too high, the output level starts to get saturated and hence rails to the supply voltage or the ground. Due to such reasons, during measurement, we were force to use low gain settings, which resulted in poor accelerometer noise. This offset is caused by the amplification on capacitance mismatch between MEMS sensor electrodes or evaluation board. To address this problem and thus achieve low-noise performance, the interface circuit requires a calibration block, which operation is discussed on following section.

3.3 Offset Calibration Circuit Design

3.3.1. Effect of Capacitance Mismatch

Most of the MEMS accelerometers employ a differential sensing as it suppresses unwanted common-mode signals, such as large static capacitance, substrate coupling, and temperature variation. This scheme is operated under assumption that all the static capacitances are identical, so that only its differential change that is caused by the actual acceleration is converted into an electrical signal. However, due to the process variation during fabrication or additional parasitic capacitance, considerable amount of capacitive mismatch exists. Such imbalances are interpreted as unwanted differential capacitance that does not change with applied acceleration, and amplified as a constant offset by the circuit gain. Previously, the transfer function of the accelerometer interface circuit was derived (equation (3-15)), based on the assumption that all the static capacitances are identical each other $(C_{S1}=C_{S2}=C_{S3}=C_{S4}=C_S)$. However, once the mismatch condition $(C_{S1} \neq C_{S2} \neq C_{S3} \neq$

C_{S4}) is included, the overall transfer function gets modified as equation (3-27), showing that any capacitive mismatch also gets converted into an offset voltage. Revised transfer function is in good agreement with the measurement result on Figure 3. 16, which shows increasing offset level with the higher circuit gain.

$$\therefore \Delta V_{OUT} = -\frac{0.5VDD}{C_F}\Delta C_{accel} - \frac{0.5VDD}{C_F}(C_{S1} - C_{S2} + C_{S3} - C_{S4}) \qquad (3\text{-}27)$$

Such behavior directly degrades the achievable dynamic range of accelerometer, especially when the amount of mismatch is similar or larger than the differential capacitance change (ΔC_{accel}). For example, the effect of mismatch is relatively low for an accelerometer with large proof-mass [12], [42], as its capacitive sensitivity (~1pF/g) is far higher than the capacitive mismatch (~100 fF/g). However, when it comes to a modern accelerometer, which has stringent requirement on the sensor form-factor, it becomes a serious problem as the reduction in proof-mass size would result in decrease in capacitive sensitivity (equation (2-6)). However, at the same time, the amount of mismatch remains unaffected as it is mostly caused due to the surrounding parasitic such as wire-bonds or package. Consequently, the offset level would be far larger than the device sensitivity and significantly impact on the dynamic range of the system. To address these issues, calibration circuit is required to suppress any non-ideal capacitive mismatch on MEMS.

Several calibration techniques have been reported to address the offset problem. A straightforward solution is to apply a separate calibration signals to the difference differential amplifier (DDA) as shown on Figure 3. 17 [64] so that its offset level can be trimmed into desire value. Still, as the calibration signal needs to be within the range of saturation region of the transistor, the calibration range is relatively narrow.

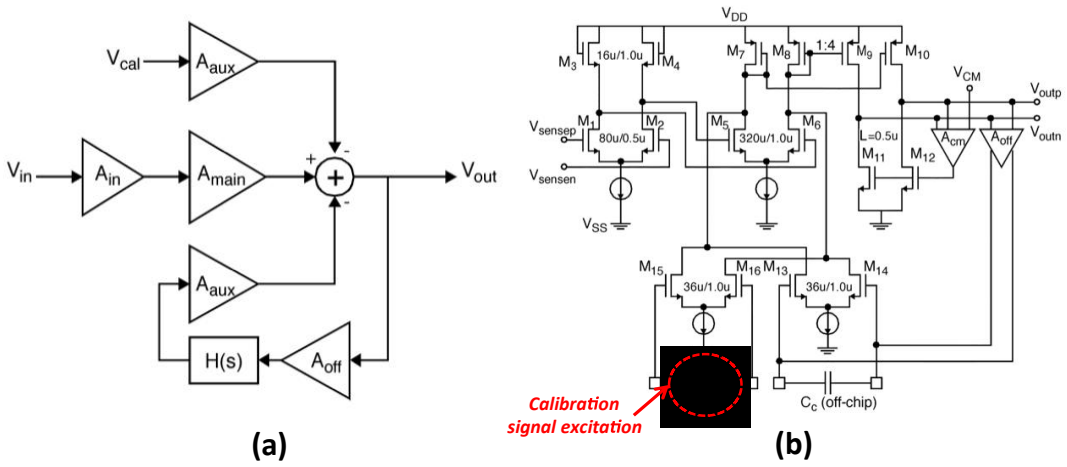


Figure 3. 17 : (a) Signal diagram and (b) schematic of differential difference amplifier (DDA) used in offset calibration

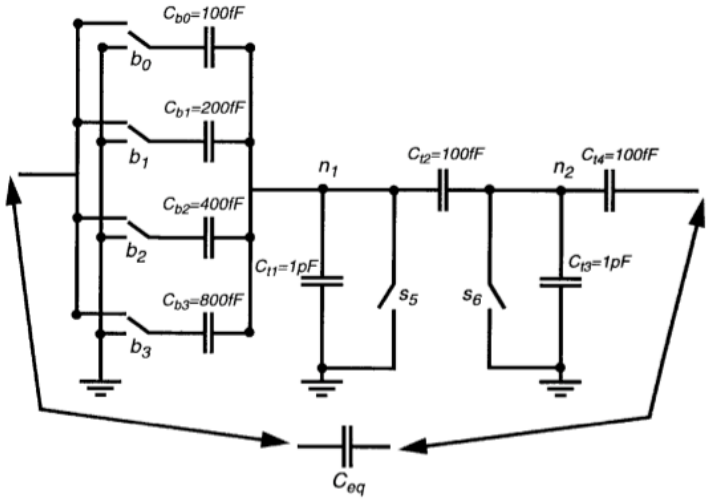


Figure 3. 18: Schematic of binary weighted capacitor bank combining series and parallel connection of transistors [65]

Another approach is to add a binary weighted capacitor bank parallel with the sensor [76] and trim its value to null out any non-ideal imbalance between MEMS capacitances. Due to its simplicity and wide calibration range, such method has been favored in many accelerometer interface circuits. Especially, by combining series and parallel connection between capacitor as shown in Figure 3. 18, the resolution level can be

dropped down to even less than 1 fF [65]. However, this configuration requires a large silicon area to integrate lager number of capacitors. Furthermore, careful layout is required to minimize parasitic capacitances between routing metals and integrated capacitors.

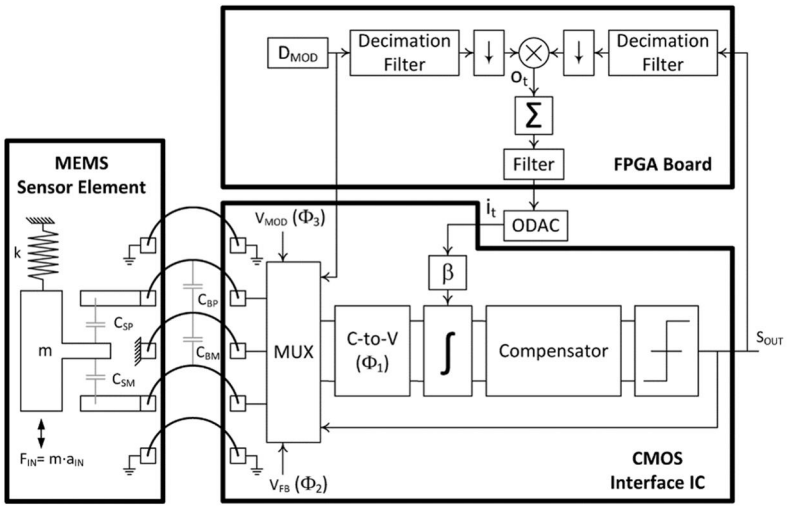


Figure 3. 19: Block diagram of the closed-loop accelerometer interface utilizing offset cancellation loop [77]

Lajevardi [77] introduced a new approach, which electrostatically modulates the spring constant of the sensor and continuously nulling out the offset level via closed-loop network. Although their method can achieve offset level reduction of 54 dB, it still has other limitation that it can only be applied for closed-loop configuration. Considering most of the commercial accelerometers are open-loop architecture, proposed method may not be effective in actual applications.

3.3.2. CHARGE-TUNING CALIBRATION

To overcome the number of issues associated with existing calibration approaches, a novel method, which utilizes controllable charges to cancel out the mismatches in MEMS sensor, is proposed [78]. Figure 3. 20 shows the basic operation, where only the half circuit is shown for simplicity. During charging phase ($\Phi_1=1$, $\Phi_2=0$), the offset capacitor (C_{offset}) is tied to the calibration voltage (V_{CAL}), storing the charges equivalent to $Q_{CAL}=C_{offset}\times V_{CAL}$. The MEMS capacitors, C_1 and C_2 are charged with supply voltage VDD and VSS as in the regular operation. Stored charges on those capacitors are equivalent to $Q_1=0.5VDD\times C_1$ and $Q_2=0.5VDD\times C_2$. On consecutive amplification phase ($\Phi_1=0$, $\Phi_2=1$), charged capacitors, C_1, C_2, and C_{offset}, are tied together at summing node, which is close to V_{CMN} level as shown on equation (3-12). As voltage potential across each capacitor is zero, stored charges would be transferred to the feedback capacitor C_F. Based on the law of charge conservation, the transfer function is derived as equation (3-28).

$$V_{OUT} = V_{accel} + V_{calibration} = \frac{0.5VDD}{C_F}\Delta C + \frac{C_{offset}}{C_F}(V_{CAL} - V_{CMN}) \quad (3\text{-}28)$$

By changing the voltage V_{CAL}, the amount of calibration charge Q_{CAL} can be trimmed and used to cancel out the excessive mismatches between MEMS capacitors. The resolution of the proposed method is dependent on the step size of calibration voltage, which has finer tuning capability compare to capacitor bank array [76]. For example, achieving 1 fF resolution level using capacitor array is a challenging task as the minimum MIM (Metal-Insulator-Metal) capacitance provided by the standard CMOS process is between 30 ~ 40 fF. However, when proposed charge calibration technique is used, only 100 fF offset capacitor and step size of 10 mV is required, which can be easily done.

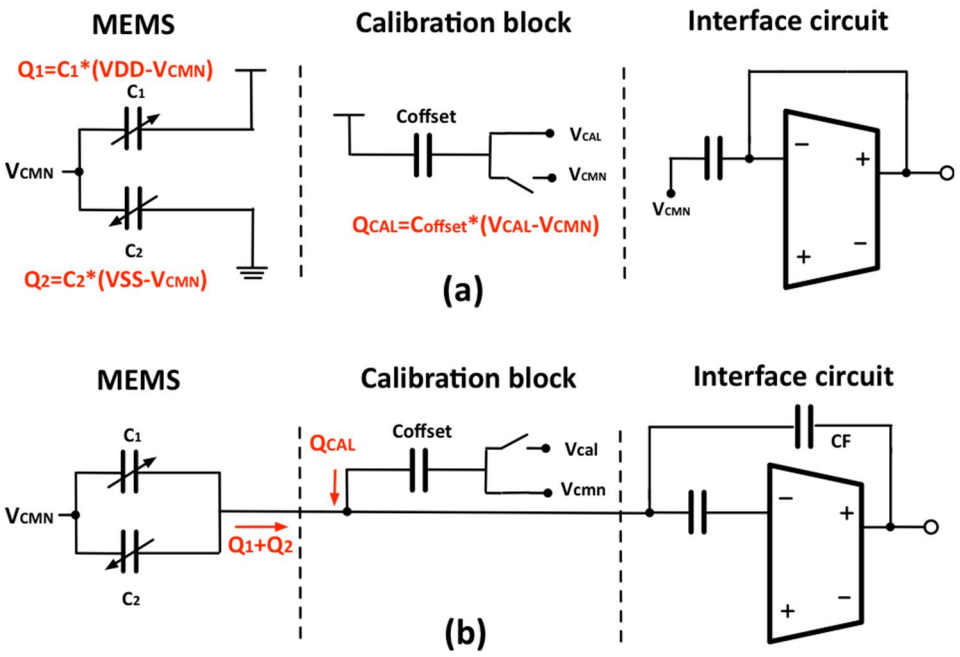


Figure 3. 20: Operation of charge-based offset calibration during (a) charging and (b) amplification phase

3.3.3. MEASUREMENT RESULT

The functionality of the proposed method is verified by creating a custom-built printed-circuit-board (PCB) that incorporates readout ASIC, and switching network with tunable capacitor, which can be trimmed from 300 fF to 1.5 pF. Both the overall schematic and photograph of implemented circuit are shown in Figure 3. 21. The MEMS accelerometer is wire-bonded to the readout ASIC, and the capacitance mismatch of the device is suppressed using proposed charge calibration method. External voltage supply is used to trim the calibration voltage V_{CAL}, which bias level can be swept from 0 to 5 V with step size of 10 mV. Figure 3. 22 (a) shows the output of the interface ASIC, when different calibration voltages V_{CAL} from 350 mV to 410 mV were applied. As can be seen from the waveform, the SC-amplifier output shows a staircase-like response with respect to calibration voltages, meaning that depending on the V_{CAL}, amount of capacitance mismatch

can be adjusted. The step size between each output level is around 20 mV, which corresponds to capacitive resolution level of 0.8 fF (CV_{gain} = 30 mV/fF).

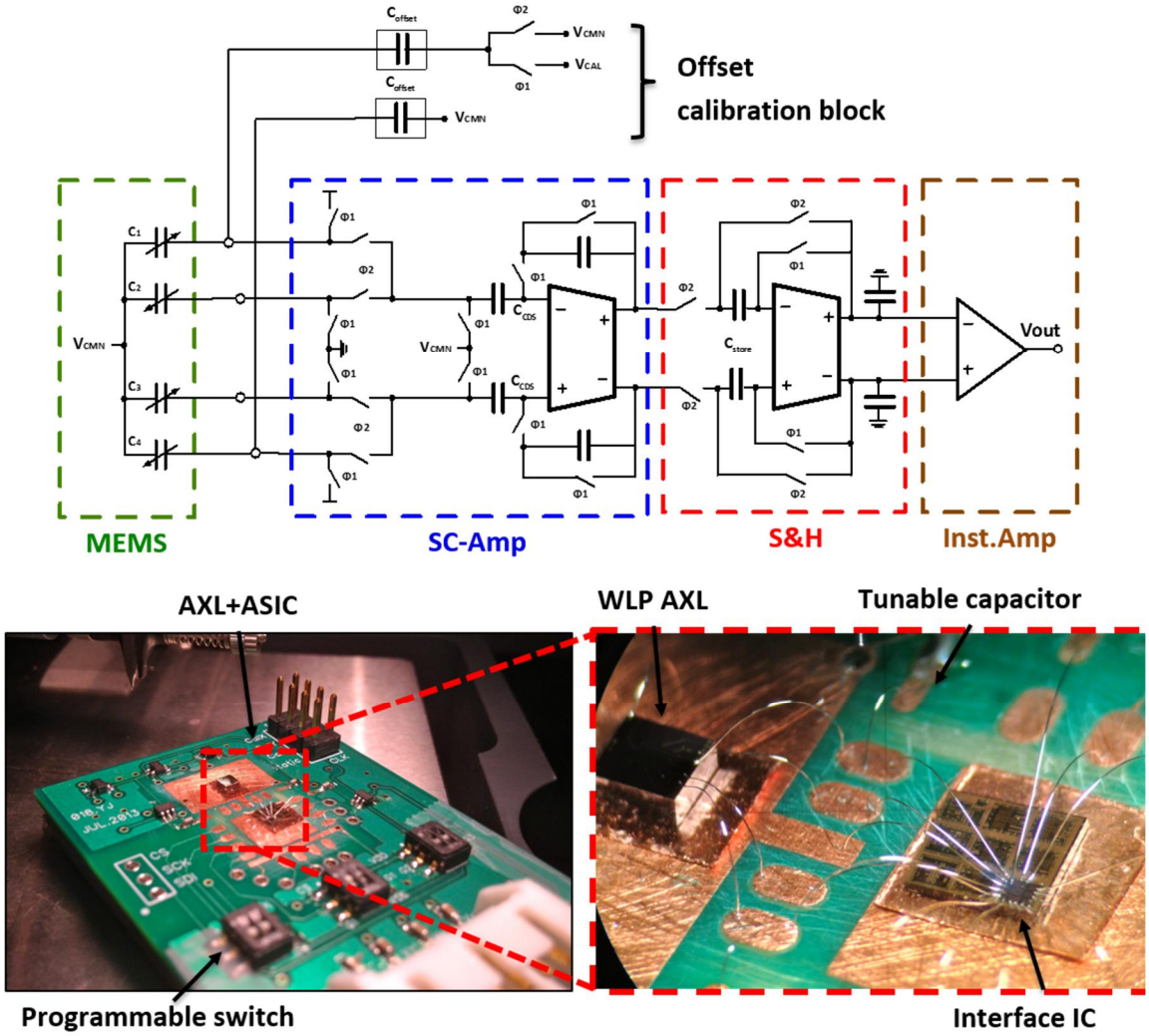


Figure 3. 21: Schematic diagram (Top) and micro-photograph (b) of evaluation board with offset calibration circuit (Bottom)

Suppressing the capacitance mismatch of the accelerometer eliminates the large offset level at the output, so that its dynamic range can be extended. This enables selecting higher gain setting for the interface circuit, and achieves improved signal-to-noise ratio. Measurement results on Figure 3. 22(b) and Figure 3. 23 shows that once the mismatches are calibrated, the sensor sensitivity can reach 270 mV/g, which is about 10 times of

improvement compared to uncalibrated sensor (=30 mV/g). Before calibration, achieving such high sensor sensitivity was impossible due to the excessive offset level.

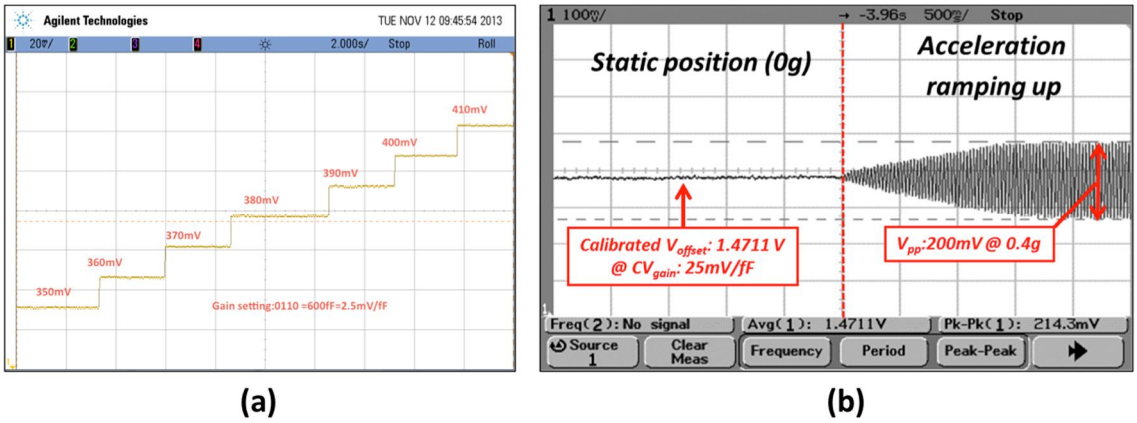


Figure 3. 22: Measurement output on (a) different calibration voltage and (b) under ramping acceleration after calibration procedure

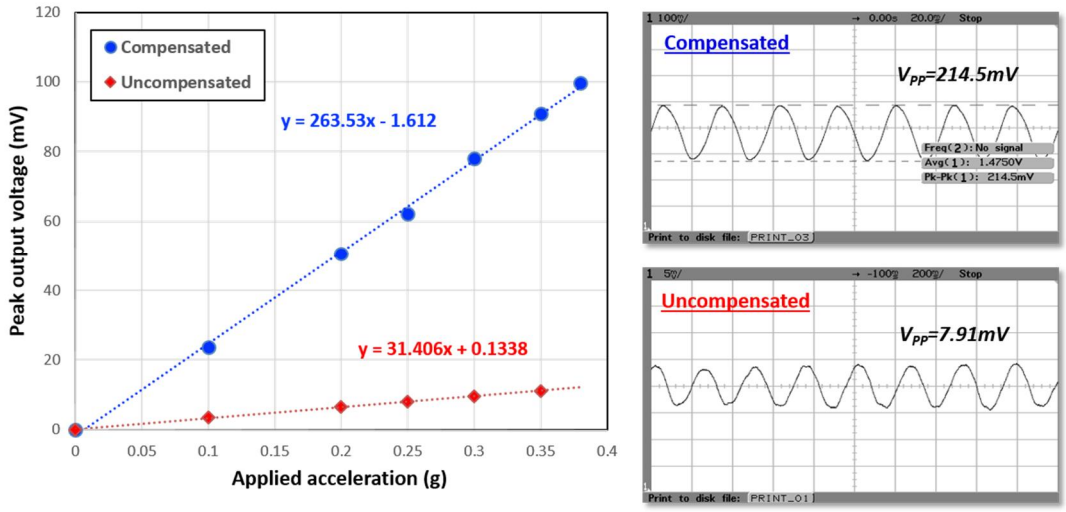


Figure 3. 23: Measured scale-factor (Left) and output waveform (Right) between compensated and uncompensated condition

Figure 3. 24(a) plots the measured noise density level between the calibrated and uncalibrated accelerometer. After the correction process, noise density level increases by 5 dB, mainly due to the noisy external voltage supply that the generates calibration voltage V_{CAL}. Figure 3. 24(b) shows the noise level of the external voltage supply itself, which is -70 dBVrms/√Hz at 1 Hz. By switching the voltage source with lesser voltage, far improved

performance can be achieved. Overall performance summary before and after the calibration is shown on Table 3. 2. Although the degradation on noise floor was observed, by utilizing proposed calibration method, the resolution level improves more than 5 times.

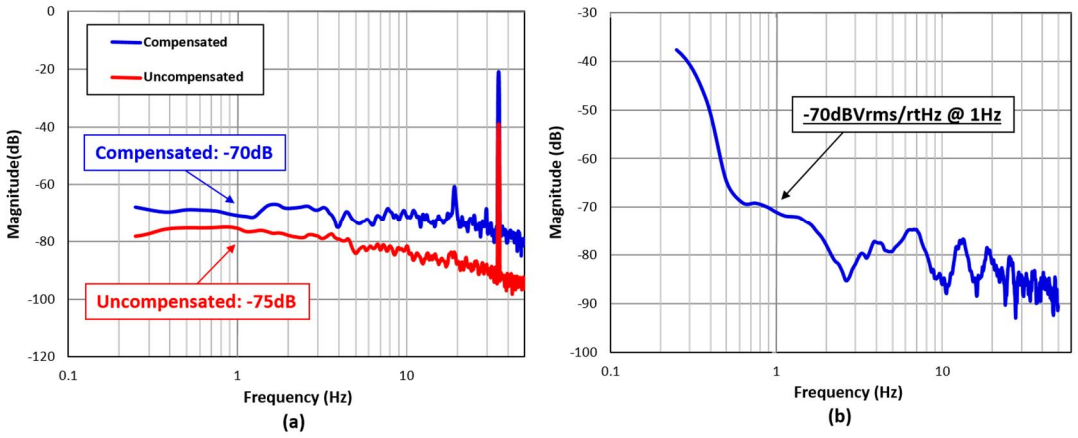


Figure 3. 24: Measured (a) noise density level spectrum between compensated and uncompensated conditions and (b) noise density level of calibration voltage *(V_{CAL})*

Table 3. 2: Performance summary

Performance metric	After calibration	Before calibration
Sensitivity	271.5 mV/g	31.4 mV/g
Circuit gain	26.4 mV/fF	3.053 mV/fF
Offset from V_{CMN} (=1.5V)	24.8 mV	263 mV
Residual capacitive mismatch	0.939 fF	86.14 fF
Noise density level	-70 $dBV_{rms}/\sqrt{Hz}$	-75 $dBV_{rms}/\sqrt{Hz}$
Resolution level	1.164 mg/√Hz	5.663 mg/√Hz

4. LOW-NOISE LOW-OFFSET MEMS ACCELEROMETER SIGNAL CONDITIONING CIRCUIT

The design and implementation of readout circuit for MEMS accelerometer is presented in prior section. Although the characterization results proved the operation of the readout circuit, several issues were also observed. First, the total noise of the accelerometer is still dominated by the electronics, resulting in poor performance than expected. To address such problem, detailed noise analysis and proper adjustment on the readout circuit is required. Secondly, the capacitance mismatch between sensor electrodes is amplified by the circuit gain and translated into huge offset level, limiting the dynamic range of the system. Although calibration technique using charge-tuning has been proposed, the method still showed poor noise performance due to external voltage supply. Such problem can be resolved by integrating all the calibration blocks into the interface circuit.

In this section, design and characterization of an accelerometer readout circuit, which overall block diagram is depicted on Figure 4. 1 is presented. Following chapter starts by analyzing the dominant noise source of the SC interface circuit for accelerometer, and adjusting the design of analog front-end block accordingly to minimize the circuit noise. The analog front-end block has precision offset and temperature calibration block, which uses novel time-averaged charge-tuning approach to suppress unwanted environmental non-idealities on MEMS devices. Furthermore, continuous-time ΣΔ modulator is incorporated after the analog front-end block so that acceleration signal can be digitized. The channel multiplexer before the analog front-end block enables the sensing of multiple

MEMS devices *(X/Y/Z-axis)* using single readout circuits. The following readout circuit is interfaced with MEMS accelerometer, and its performances are characterized.

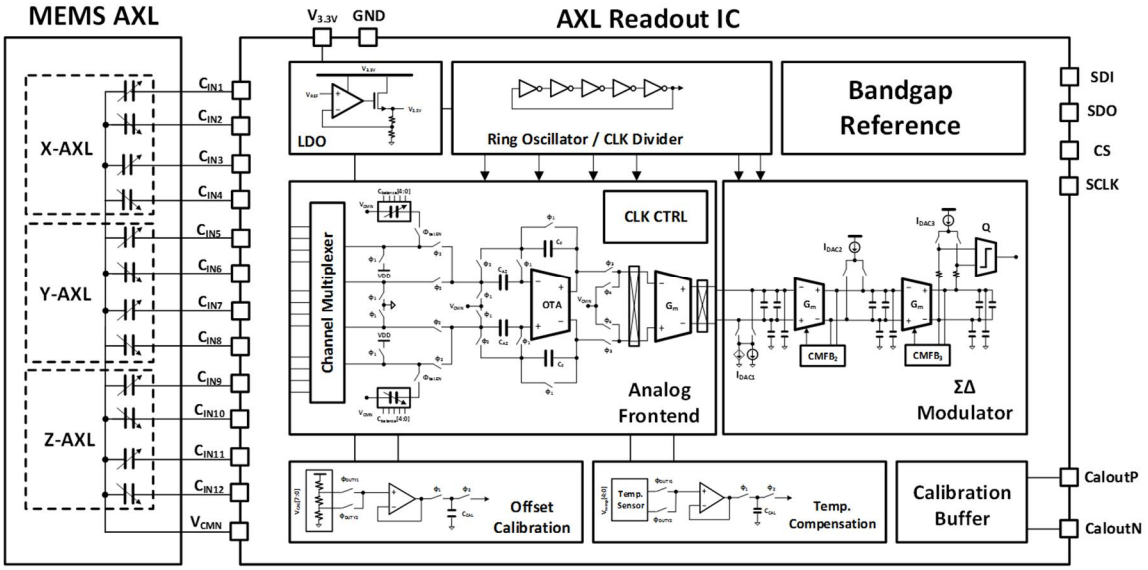


Figure 4. 1: System diagram of accelerometer interface circuit

4.1 CIRCUIT NOISE INVESTIGATION

From the *CNEA* expression on equation (2-12), it is concluded that there are mainly two ways to improve the circuit noise. One method is to increase the capacitive sensitivity of MEMS accelerometer by modifying device geometry (e.g. large proof-mass *(M)*, low stiffness *(K),* or smaller sensing gap *(d)*). However, this may not be always feasible due to the limitation on the fabrication process or requirement on device size. The other approach is to reduce the capacitive resolution, ΔC_{min}, which is equivalent to the output noise of the circuit $(V_{n.out})$ divided by its capacitance-to-voltage gain (CV_{gain}). However, even though several researches have been conducted so far, ΔC_{min} was often considered as a *"black box"* and arbitrary numbers (0.5~1 aF/√Hz) were used instead [67], [79]. This is mainly because there are so many noise sources inside the circuit that affects the overall performance [66],

and becomes hard to distinguish the major contributors. In this section, a detailed noise analysis will be conducted to determine the dominant noise source.

4.1.1. NOISE ANALYSIS OF ACCELEROMETER INTERFACE CIRCUIT

As the entire accelerometer interface circuit is consisted of number of different sub-blocks, such as SC-amplifier, G_m-cell, and ΣΔ modulator as shown in Figure 4. 1, analyzing the entire noise performance would be a cumbersome task. Such difficulty can be mitigated by using Friis formula, which is expressed as equation (4-1) [80]. F_{total} indicates the noise factor of the entire system, F_i and G_i are the noise factor and gain of the *i*-th stage, and *n* is the number of stages, respectively. The key message of the Friis formula is that the noise of the entire system is dominated by the first stage, which is the SC-amplifier in accelerometer interface circuit [81]. Therefore, in following analysis, we will be focusing mainly on the noise of SC-amplifier.

$$F_{total} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \frac{F_4 - 1}{G_1 G_2 G_3} + \ldots + \frac{F_n - 1}{G_1 G_2 \cdot\cdot G_{n-1}} \qquad (4\text{-}1)$$

The overall noise of the SC-amplifier can be evaluated by combining noise at each phase; charging *(Φ_1=1, Φ_2=0)* and amplification *(Φ_1=0, Φ_2=1)* phases as equation (4-2).

$$\overline{V_n}^2 = \overline{V_{n.out.\phi 1}}^2 + \overline{V_{n.out.\phi 2}}^2 \qquad (4\text{-}2)$$

To evaluate the noise at charging phase *(Φ_1=1, Φ_2=0)*, the noise model of the SC amplifier*)* is depicted as Figure 4. 2. To ease the analysis, the original SC-amplifier connection on Figure 3. 4 is simplified as half circuit and CDS capacitor to suppress 1/f noise is omitted. C_1 and C_2 represent the static capacitance of the MEMS accelerometer.

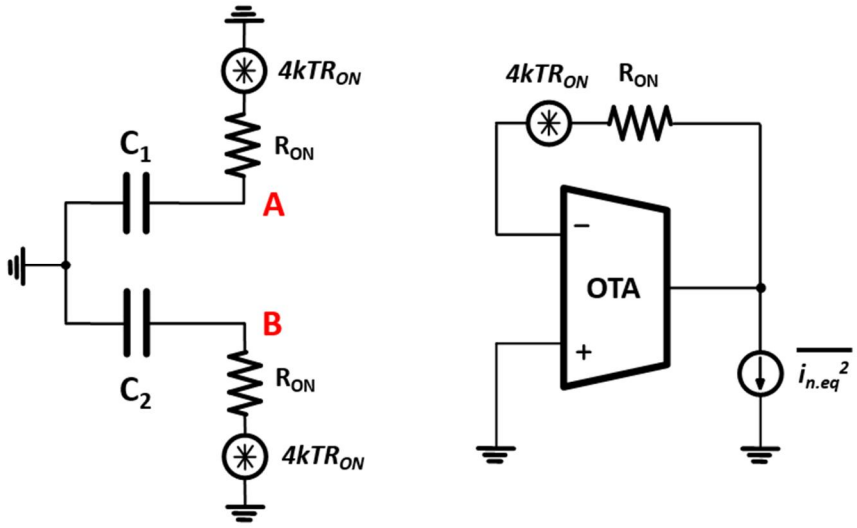


Figure 4. 2: Noise model of SC-amplifier during charging phase *(Φ_1=1, Φ_2=0)*

When both MEMS capacitors are tied to the either of supply voltage or ground, thermal noise of the on-state resistance on each switch gets stored on C_1 and C_2, resulting kT/C noise at node A and B as expressed as equation (4-3). Stored noise charges are expressed as equation (4-4).

$$\overline{V_{n.A}^2} = \frac{kT}{C_1}, \quad \overline{V_{n.B}^2} = \frac{kT}{C_2} \tag{4-3}$$

$$\overline{Q_{n.A}}^2 = C_1^2 \cdot \overline{V_{n.A}}^2 = kTC_1, \quad \overline{Q_{n.B}}^2 = C_2^2 \cdot \overline{V_{n.B}}^2 = kTC_2 \tag{4-4}$$

The noise of the OTA under unity gain feedback configuration is calculated by integrating OTA equivalent noise current $\overline{i_{eq}}^2$, and its output resistance R_{eq}^2 with respect to the frequency. Note that there is another switch, which also has on-state resistance R_{ON} that shorts input and output of the OTA, creating an additional thermal noise $(4kTR_{ON})$. The total output noise during charging phase $(\Phi_1=0, \Phi_2=1)$ is expressed as equation (4-5).

$$\overline{V_{n.\phi 1}^2} = \overline{V_{n.OTA}^2} = \int_0^\infty (4kTR_{ON} + \overline{i_{eq}}^2 R_{eq}^2)\, df \tag{4-5}$$

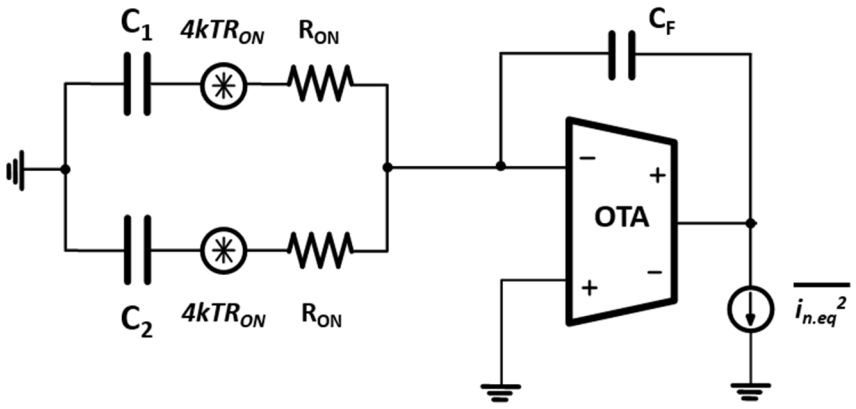


Figure 4. 3: Simplified noise model of SC-amplifier during amplification phase *(Φ_1=0, Φ_2=1)*

During amplification phase *(Φ_1=0, Φ_2=1)*, MEMS capacitors C_1 and C_2 are tied each other, transferring stored charges into the feedback capacitor C_F as shown in Figure 4. 3. By the law of charge conservation, stored noise charge shown in equation (4-4) is referred to output by dividing with feedback capacitor C_F (equation (4-6)).

$$\overline{V_{n.out.MEMS}}^2 = \frac{1}{C_F^2}\left(\overline{V_{n.A}}^2 + \overline{V_{n.B}}^2\right) = \frac{kT}{C_F^2}\left(C_1 + C_2\right) \qquad (4\text{-}6)$$

The output noises from the switch and the OTA are calculated by integrating each noise component, $S_{switch}(f)$ and $S_{OTA}(f)$ with its transfer function $H(f)$ as shown in equation (4-7) to (4-9).

$$S_{switch}(f) = 4kTR_{ON}, \quad S_{OTA}(f) = \overline{i_{eq}}^2 \cdot R_{eq}^2, \quad H(f) = \frac{A_{CL}}{1 + j2\pi f \cdot R_{eq}C_{eq}} \qquad (4\text{-}7)$$

$$\overline{V_{n.out.switch}}^2 = \int_0^\infty 4kTR_{ON}\left|\frac{A_{CL}}{1 + j2\pi f \cdot R_{eq}S_{eq}}\right|^2 df = \frac{kTR_{ON}A_{CL}^2}{R_{eq}C_{eq}} \qquad (4\text{-}8)$$

$$\overline{V_{n.out.OTA}}^2 = \int_0^\infty \overline{i_{eq}}^2 R_{eq}^2 \cdot \left|\frac{A_{CL}}{1 + sR_{eq}S_{eq}}\right|^2 df = \frac{\overline{i_{eq}}^2}{4C_{eq}^2} \qquad (4\text{-}9)$$

By adding each noise component, the output noise during amplification phase *(Φ_1=0, Φ_2=1)* is calculated as equation (4-10).

$$\overline{V_{n.out.\phi 2}}^2 = \frac{kT}{C_F^{\,2}}(C_1 + C_2) + \frac{kTR_{ON}A_{CL}^{\,2}}{R_{eq}C_{eq}} + \frac{\overline{i_{eq}}^2}{4C_{eq}^{\,2}} \qquad (4\text{-}10)$$

Finally, the total output noise can be expressed as equation (4-11) by merging the noise at charging phase (equation (4-5)) and at amplification phase (equation (4-10)).

$$\overline{V_{n.out}}^2 = \int_0^\infty (4kTR_{ON} + i_{eq}^{\,2}R_{eq}^{\,2})df + \frac{kT}{C_F^{\,2}}(C_1 + C_2) + \frac{kTR_{ON}A_{CL}^{\,2}}{R_{eq}C_{eq}} + \frac{\overline{i_{eq}}^2}{4C_{eq}^{\,2}} \qquad (4\text{-}11)$$

The equation (4-11) can be simplified by assuming 1/f noise of the OTA will be suppressed using noise cancellation techniques, such as CDS or chopper stabilization [63]. As mentioned earlier, the CDS capacitor was intentionally removed in Figure 4. 2 and Figure 4. 3 to simplify the analysis. By doing so, the lumped noise component i_{eq}^2 of the OTA can be opted out and overall noise expression will be simplified as equation (4-12).

$$\overline{V_{n.out}}^2 \approx \frac{kT}{C_F^{\,2}}(C_1 + C_2) + \frac{kTR_{ON}}{R_{eq}C_{eq}}A_{CL}^{\,2} \qquad (4\text{-}12)$$

Equation (4-12) is consisted of two components; *kT/C* noise coming from the amplifier, and thermal noise from the transistor switch. To determine which component has larger effect on overall noise, its ratio was compared as shown in equation (4-13).

$$\frac{Noise@kT/C}{Noise@thermal} = \frac{\frac{kT}{C_F^{\,2}}(C_1 + C_2)}{\frac{kTR_{ON}}{R_{eq}C_{eq}}A_{CL}^{\,2}} = \frac{R_{eq}C_{eq}(C_1 + C_2)}{R_{ON}C_F^{\,2}A_{CL}^{\,2}} \qquad (4\text{-}13)$$

By replacing A_{CL}, R_{eq}, and C_{eq} with equation (4-14) to (4-25), the equation (4-13) is derived as equation (4-16).

$$A_{CL} = \frac{A_{OL}}{1 + A_{OL}\beta} \approx \frac{1}{\beta} = \frac{C_1 + C_2}{C_F},\ R_{eq} = \frac{1}{g_m \beta} = \frac{C_1 + C_2}{g_m C_F} \qquad (4\text{-}14)$$

$$C_{eq} = C_L + \frac{C_F \cdot (C_{S1} + C_{S2})}{C_F + C_{S1} + C_{S2}} \approx C_L + C_F \qquad (4\text{-}15)$$

$$\frac{Noise@kT/C}{Noise@thermal} = \frac{C_L + C_F}{C_F} \frac{1}{R_{ON} g_m} \qquad (4\text{-}16)$$

As the on-state resistance *(R_{ON})* of the transistor switch is relatively low, and the transconductance g_m is between mS to μS range, it can be concluded that the SC-amplifier noise is mostly dominated by the *kT/C* noise of the MEMS accelerometer as expressed in equation (4-17).

$$\overline{V_{n.out}}^2 \approx \frac{kT}{C_F^{\,2}} (C_1 + C_2) \qquad (4\text{-}17)$$

The SC-amplifier output is a sampled output, which causes high frequency noise components to be aliased back to the lower frequency bandwidth as shown in Figure 4. 4. Such phenomena, which is called as noise folding [82], causes the accelerometer noise density level to increase significantly as expressed in equation (4-18). f_{SW} represents the operational clock frequency of the SC-amplifier, and C_{MEMS} as the sum of static capacitance at MEMS accelerometer respectively *($C_{MEMS}=C_1+C_2$)*.

$$S(f) = \frac{1}{C_F} \sqrt{\frac{kTC_{MEMS}}{f_{sw}/2}}\ \ [V/\sqrt{Hz}] \qquad (4\text{-}18)$$

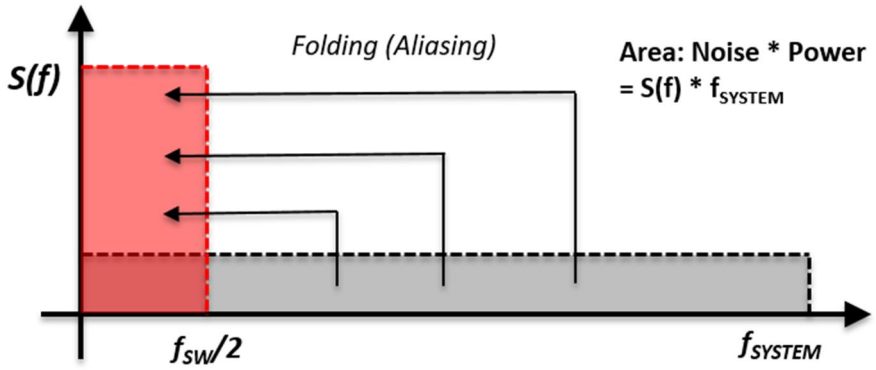


Figure 4. 4: Noise folding effect of sampled data system

Finally, the capacitive resolution ΔC_{min} in equation (2-12) can be derived as equation (4-19).

$$\Delta C_{\min} = \frac{S(f)}{CV_{gain}} = \frac{1}{0.5VDD}\sqrt{\frac{kTC_{MEMS}}{f_{SW}/2}} \quad [F/\sqrt{Hz}] \qquad (4\text{-}19)$$

This expression on circuit noise is verified using periodic noise (PNOISE) simulation using Cadence Spectre, where the simulated results are shown on both Figure 4. 5 and Figure 4. 6. It is observed that the noise density level increases with the MEMS capacitances, and decreases with the switching clock frequency (f_{SW}), which are in good agreement with the equation (4-19). Therefore, it can be concluded that to attain improved circuit noise performance for the accelerometer, low MEMS capacitance and high switching clock frequency is required. Note that such conclusion assumes 1/f noise of the OTA is fully suppressed using dynamic noise cancellation techniques. Otherwise, low-frequency noise from the OTA would dominate the entire circuit noise performance.

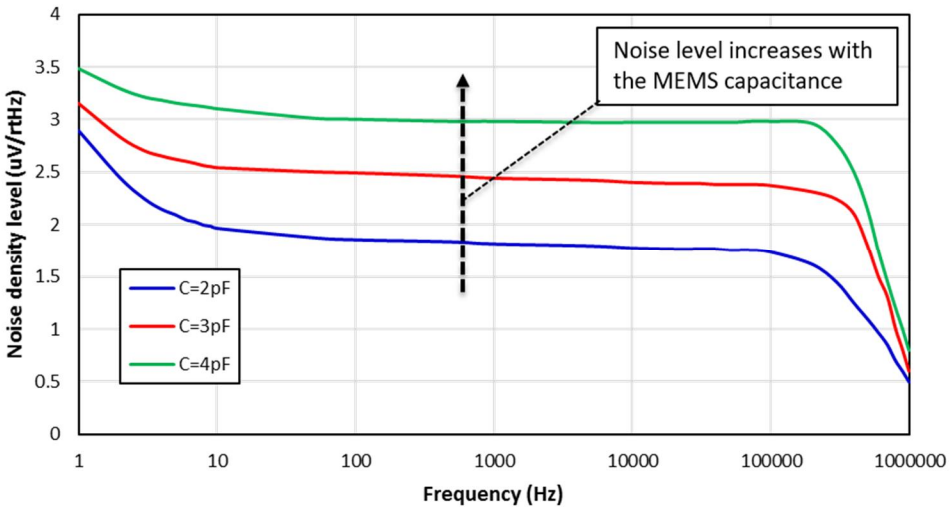


Figure 4. 5: PNOISE simulation of SC-amplifier under different MEMS capacitance

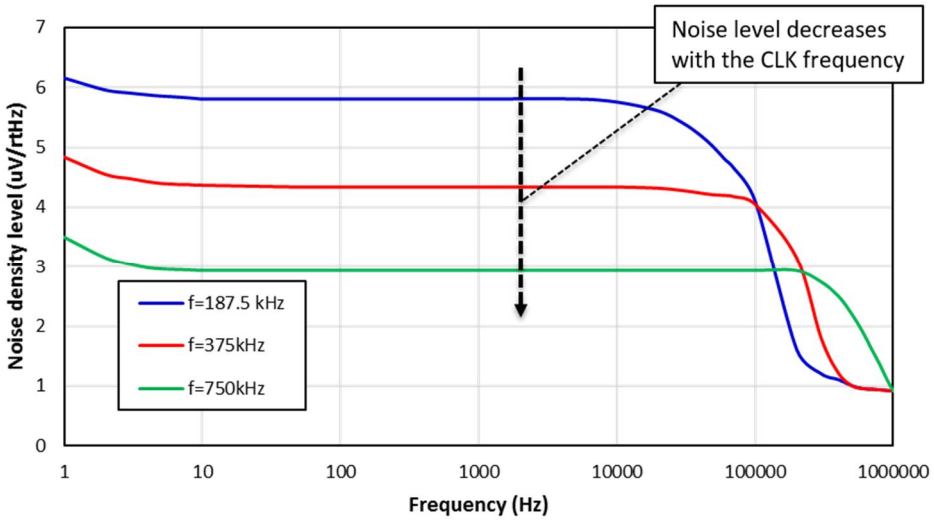


Figure 4. 6: PNOISE simulation of SC-amplifier under different clock frequency

Although equation (4-19) shows that the reduction in MEMS capacitance C_{MEMS} would lower the circuit noise, doing so also decreases overall device sensitivity as expressed on equation (2-6). Therefore, one might think lowering static capacitance on the accelerometer would deteriorate the acceleration-referred noise performance *(CNEA)*. However, it should be noted that static capacitance C_S in equation (2-6) only denotes the capacitance of the sensing electrode, whereas the MEMS capacitance C_{MEMS} in equation (4-19) incorporates all the parasitic capacitances that are parallel with sensing capacitance.

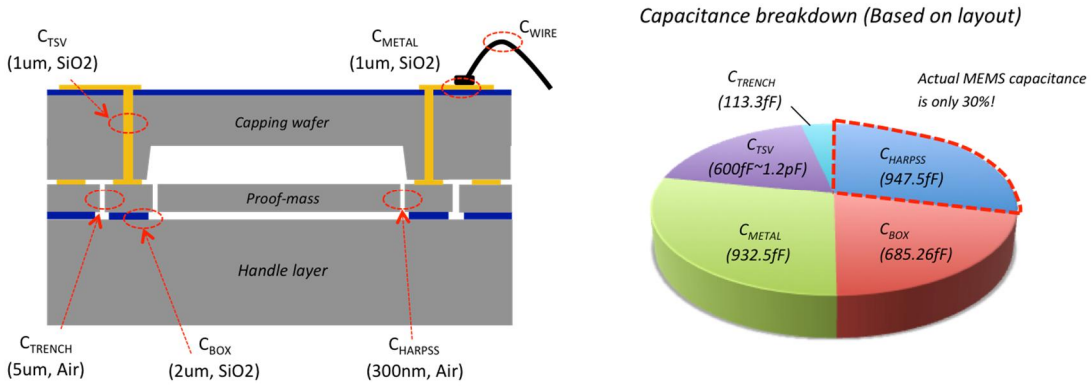


Figure 4. 7: Parasitic capacitance breakdown on MEMS accelerometer

From the cross-sectional view of the wafer-level packaged accelerometer on Figure 4. 7, it is known that there are number of parasitic capacitances (TSV, Metal traces, etc) that are parallel with the sense capacitance. The breakdown plot on Figure 4. 7 shows that those parasitic can be as large as 70 % of the entire capacitance C_{MEMS}, and does not contribute to any of the capacitive sensitivity of MEMS accelerometer, but only increases the *kTC* noise. Therefore, to lower capacitive resolution ΔC_{min}, it is important to minimize parasitic capacitance on equation (4-20) as much as possible.

$$C_{MEMS} = C_{sense} + C_{parasitic} \qquad (4\text{-}20)$$

Considering this, the circuit noise equivalent acceleration (CNEA) can be expressed as equation (4-21) by combining equation (2-12), (4-19) and (4-20).

$$CNEA = \frac{1}{0.5VDD}\sqrt{\frac{kT(C_{sense}+C_{parasitic})}{f_{sw}/2}}\cdot\frac{d}{4C_{sense}}\omega_0^2 \ [m/\sec^2/\sqrt{Hz}] \qquad (4\text{-}21)$$

4.2 ANALOG FRONT-END CIRCUIT DESIGN

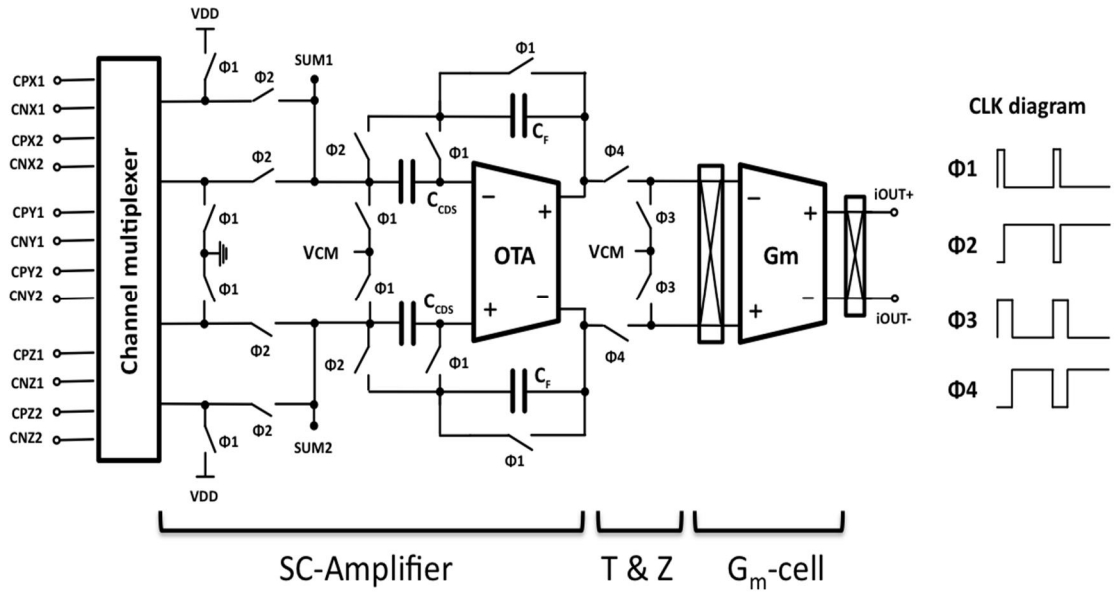


Figure 4. 8: Schematic of analog front-end block, which is consisted of channel multiplexer, SC-amplifier and G_m-cell

The schematic diagram of analog front-end block is shown on Figure 4. 8. It is consisted of channel switching multiplexer, SC-amplifier, track and zero (T&Z) switch and G_m-cell. The main objective of the analog front-end block is to convert the capacitance change from the MEMS accelerometers into an electrical signal, while maintaining low noise level. The amplified signal is then digitized using continuous time ΣΔ modulator located after the analog front-end block. Entire operation is controlled using two non-overlapping clock signals, which have uneven duty cycle *(Φ_1:Φ_2=1:7)* to allow more time for the amplified output to be settled at desired level during amplification phase (*Φ_1=0, Φ_2=1)*. The track and zero (T&Z) switch, which is added between SC-amplifier and G_m-cell, is controlled by another clock phase *(Φ_3/Φ_4)* that also has different duty cycle *(Φ_3:Φ_4=2:6)*. Offset and temperature compensation block, which are not shown in the

schematic above, are connected via summation node *(Sum1 & Sum2)* of the SC-amplifier and provides the calibration signal to suppress unwanted non-idealities.

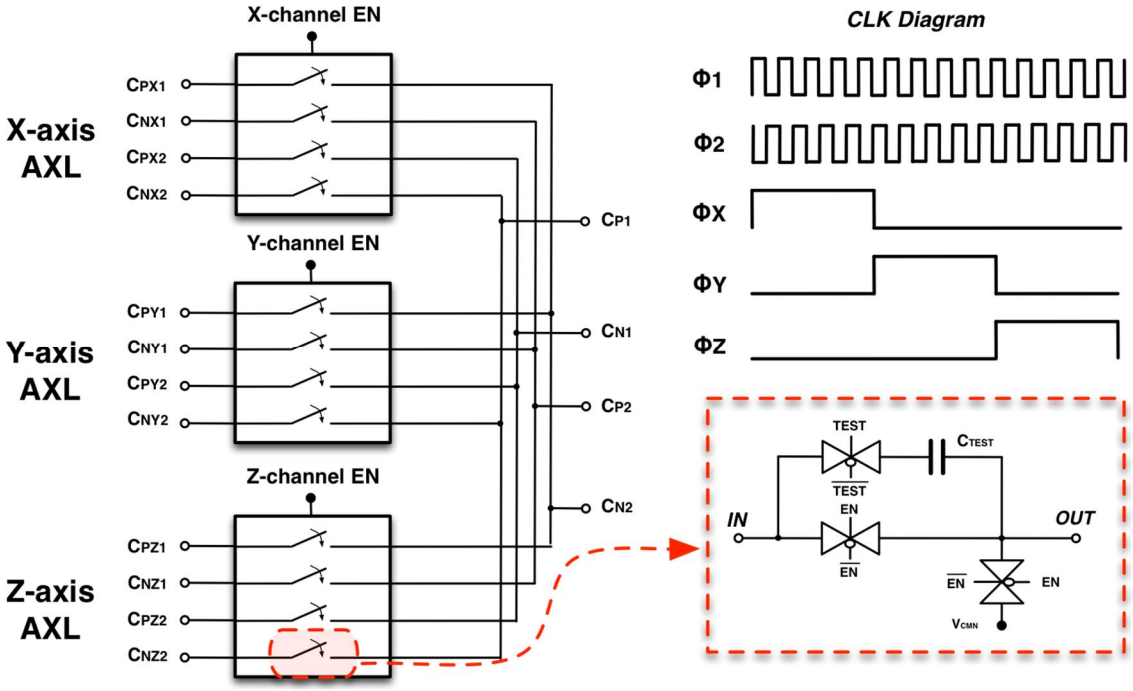


Figure 4. 9: Schematic of channel switching multiplexer and its clock-timing diagram. Each switch has a test capacitor for "circuit-only" configuration.

The schematic of the channel-switching block is shown on Figure 4. 9. When the enabling signal for each axis *(x-/y-/z-)* is set high, corresponding channel switch connects the MEMS capacitors to the input of SC-amplifier. Transmission gate switch is used to maintain low on-state resistance *(R_{ON})* regardless of the gate-source voltage on MOSFET transistors. When the channel is disabled, corresponding MEMS capacitors are connected to V_{CMN} node *(=VDD/2)* instead, creating a zero-voltage potential between the electrode and the proof-mass to eliminate the possibility of pulling-in. Additionally, each set of switches has a separate on-chip test capacitor (C_{test}=~3pF) that can be used for *"ASIC-only"* testing. Under such configuration, test capacitors *(C_{test})* are tied to the input of the SC-amplifier instead so that the circuit operation can be isolated from any possible non-

ideal effect from the MEMS sensor (temperature variation, capacitive coupling). This helps characterizing the sole-performance of the interface circuit.

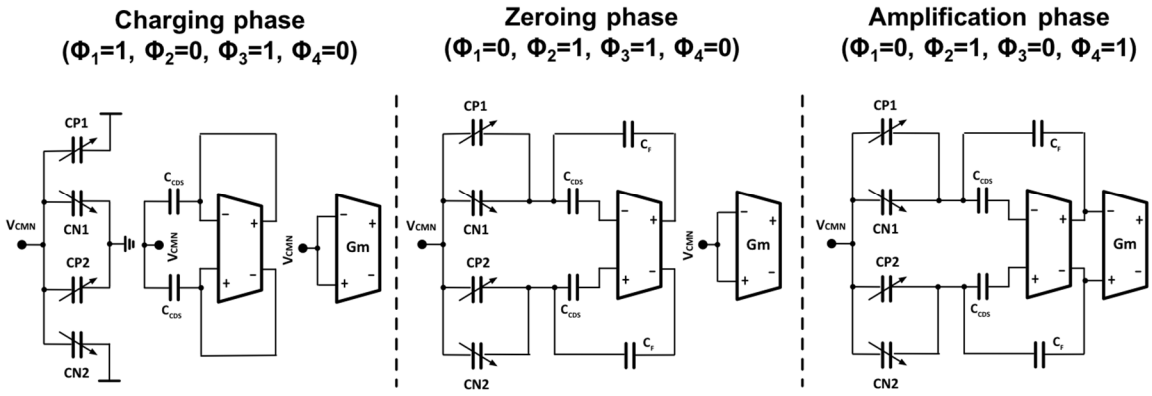


Figure 4. 10: Analog-frontend block operation under three separate clock phase

The operation of the analog front-end block is consisted of three separate phases as shown in Figure 4. 10. During charging phase *(Φ_1=1, Φ_2=0, Φ_3=1, Φ_4=0),* SC-amplifier is connected in unity-gain feedback configuration, and the track & zero switch shorts the differential inputs of the G_m-cell to the V_{CMN} node, so that the 1/f noise of OTA does not transferred to the final output. At zeroing phase *(Φ_1=0, Φ_2=1, Φ_3=1, Φ_4=0)*, the SC-amplifier converts the capacitance change of accelerometer into a differential voltage, based on the operation described in Chapter 3. However, the track & zero switch still shorts the G_m-cell input as large portion of 1/f noise is still present during settling of SC-amplifier output. At consecutive amplification phase *(Φ_1=0, Φ_2=1, Φ_3=0, Φ_4=1)*, track & zero switch connects the SC-amplifier output to G_m-cell.

Target specifications of the OTA are summarized in Table 4. 1. The interface circuit uses the clock frequency as high as 750 kHz to minimize the kTC noise. To ensure fully-settled output within the given time, it is concluded that the 3-dB bandwidth of the OTA under closed-loop configuration (C_{MEMS} = 4 pF, C_F = 80 fF)) needs to be as high as 1 MHz.

Also, to meet the non-linearity requirement (< 0.1 %), the loop-gain *(≈A_{OL}·β)* needs to be higher than 40 dB as well. This specification gives the required open-loop DC gain *(A_{OL})* of the OTA as high as 80 dB, and unity gain bandwidth product as 75 MHz.

Table 4. 1: Target specification of the OTA

Performance parameter	Target value
Supply voltage (VDD)	2.5 V
Current consumption	75 μA
Open-loop DC gain *(A_{OL})*	> 80 dB
Phase margin	> 45°
Unity gain bandwidth	75 MHz
CMFB Phase margin	> 45 °

Figure 4. 11 shows the schematic of the operational transconductance amplifier (OTA), which uses triple-cascode topology. Compared to the gain-boosted method that was previously used in Chapter 3, presented circuit has lesser power consumption and less stability issues. The DC gain of the OTA is expressed as equation (4-22).

$$A_{OL} = G_m R_{out} = g_{m2} \cdot (g_{m7} g_{m9} r_{ds7} r_{ds9} r_{ds5}) \| (g_{m2} g_{m4} r_{ds2} r_{ds4} r_{ds6}) \qquad (4\text{-}22)$$

Differential difference amplifier (DDA) is used to implement common-mode feedback (CMFB) network to achieve fully-differential operation. Additional resistors are placed at the source node of *PM14 ~ PM17* to degenerate the input transistor gain and hence improve the stability of the common-mode feedback (CMFB) loop. The simulated frequency response is shown at Figure 4. 12, where the open-loop DC gain *(A_{OL})* of 120.4 dB, the phase margin of 57.3 degree, and the unity gain bandwidth of 100 MHz satisfies the target specifications. The stability of the CMFB network was also simulated by placing

IPROBE element at the control voltage from the CMF circuit. The simulated phase margin is 81 degrees, which satisfies stability requirement.

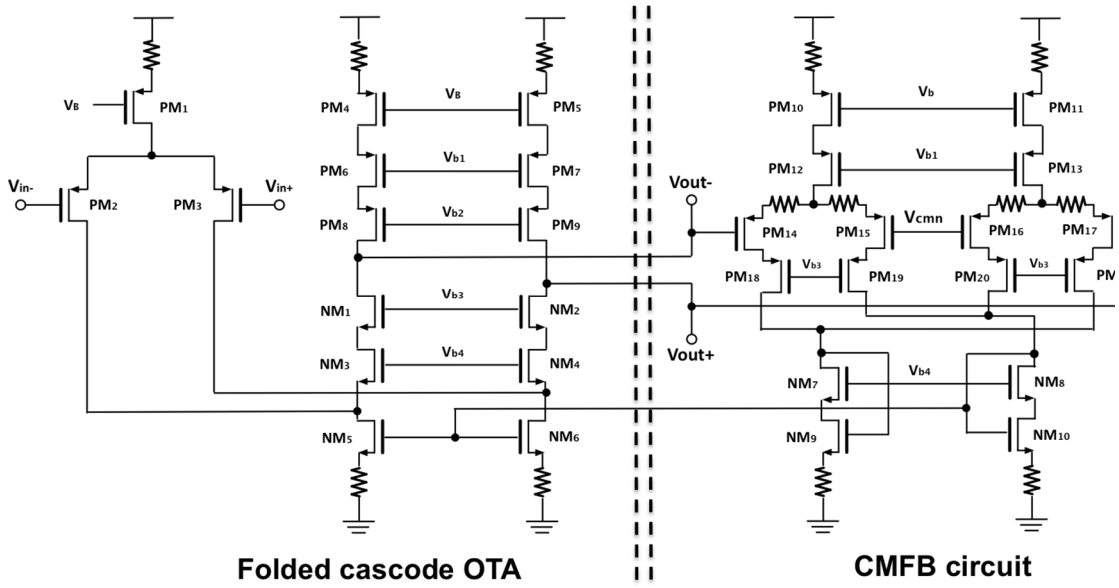


Figure 4. 11: Schematic of triple folded-cascode amplifier with CMFB circuit

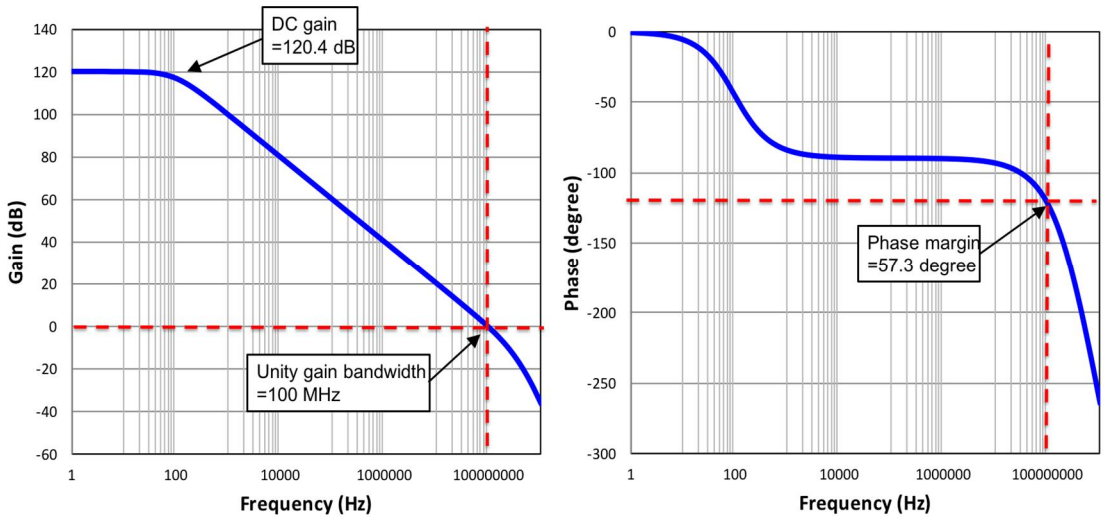


Figure 4. 12: Simulated frequency response of the fully-differential OTA showing (Left) gain and (Right) phase margin

To guarantee the robustness of the OTA under extreme conditions, AC response at different PVT (Process corner/Voltage/Temperature) conditions were also simulated.

There are 9 process corners *(tt/ss/ff/nspfrs/nspfrf/nfpsrs/nfpsrf/nspsrf/nfpfrs)*, where *"t"* represents the transistor mobility level at typical condition, *"s"* as low *(slow)*, and *"f"* as highest mobility level *(fast)* respectively. Different supply voltages (2.4V/2.5V/2.6 V) and temperature (-40 °C /27 °C /85 °C) were also used during analysis. Figure 4. 13 plots the simulated DC gain and phase margin with respect to different conditions. Worst-case result occurs at *nspfrf"* corner, 2.4 V supply voltage and temperature level of 27 °C. Still, the value (104.25 dB / 54.6 degree) value satisfies the target specification in Table 4. 1.

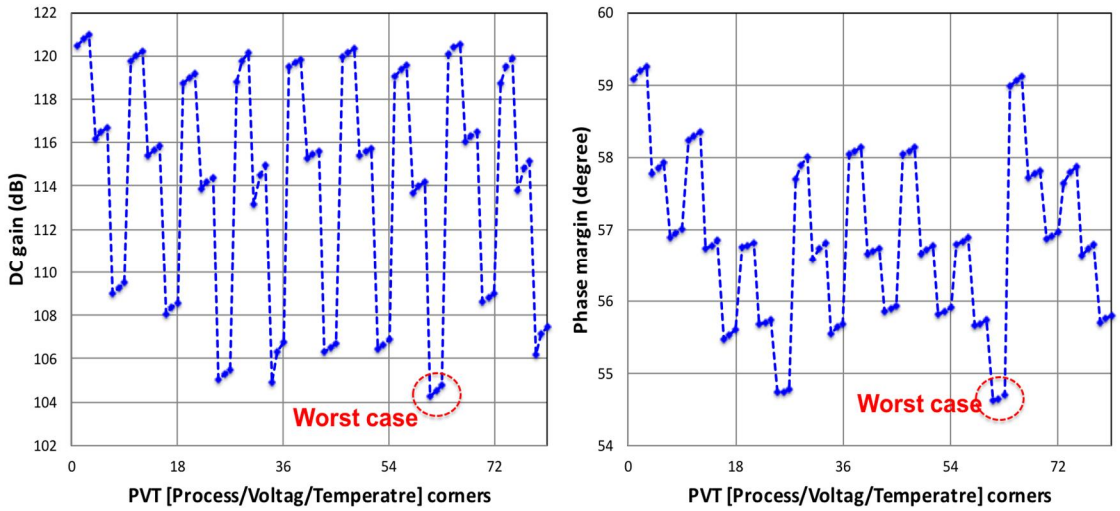


Figure 4. 13: Process corner simulation result of fully-differential OTA showing (Left) DC gain and (Right) phase margin

G_m-cell block converts the output voltage from SC-amplifier into the continuous current and feeds it into the ΣΔ modulator located after the analog front-end. The transconductance gain is controlled by the programmable feedback resistor *R* that is located between each drain of input transistors NM_{in+}, and NM_{in} (Figure 4. 14(a)). The chopping switches are added at both input and output of G_m-cell to remove 1/f noise of the transistor. Figure 4. 14 (b) shows the simulated transconductance gain under different configuration.

The bias voltages are generated using bandgap circuit and cascode current mirror [82] as shown in Figure 4. 15. The reference voltage V_{REF} from the bandgap circuit biases the gate of transistor *M1* and generates a temperature-stable current I_{REF}, which would also flow through the transistor *M3/M4* and creates bias voltages $(V_{B1}, V_{B2}, V_{B3}, \& V_{B4})$ for the OTA and other circuit blocks.

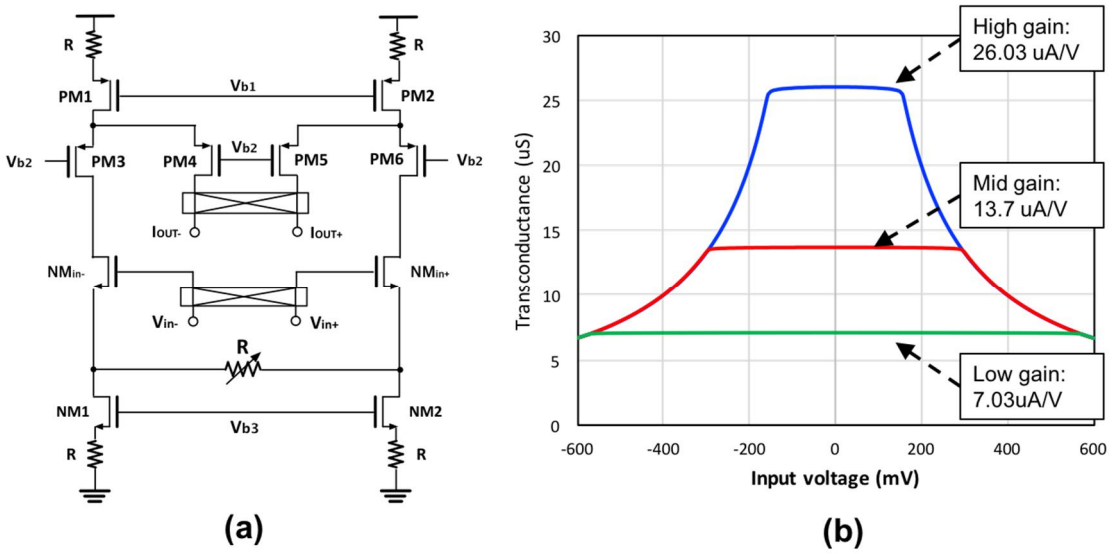


Figure 4. 14: (a) Schematic of the G_m-cell block and (b) transconductance simulation result under different gain setting

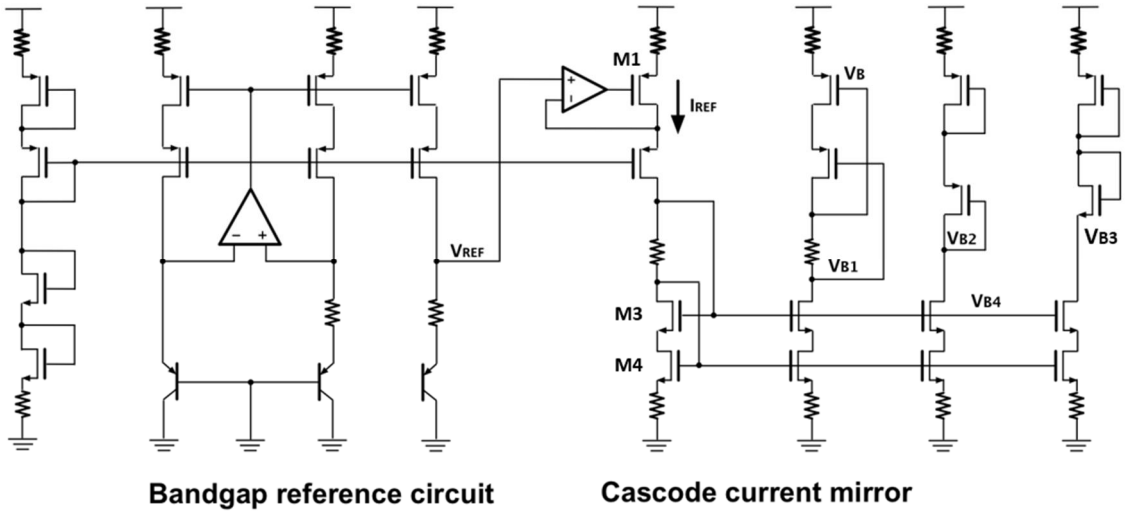


Figure 4. 15: Schematic of the bias voltage generation circuit using bandgap reference

4.3. Design of Offset and Temperature Calibration Circuit

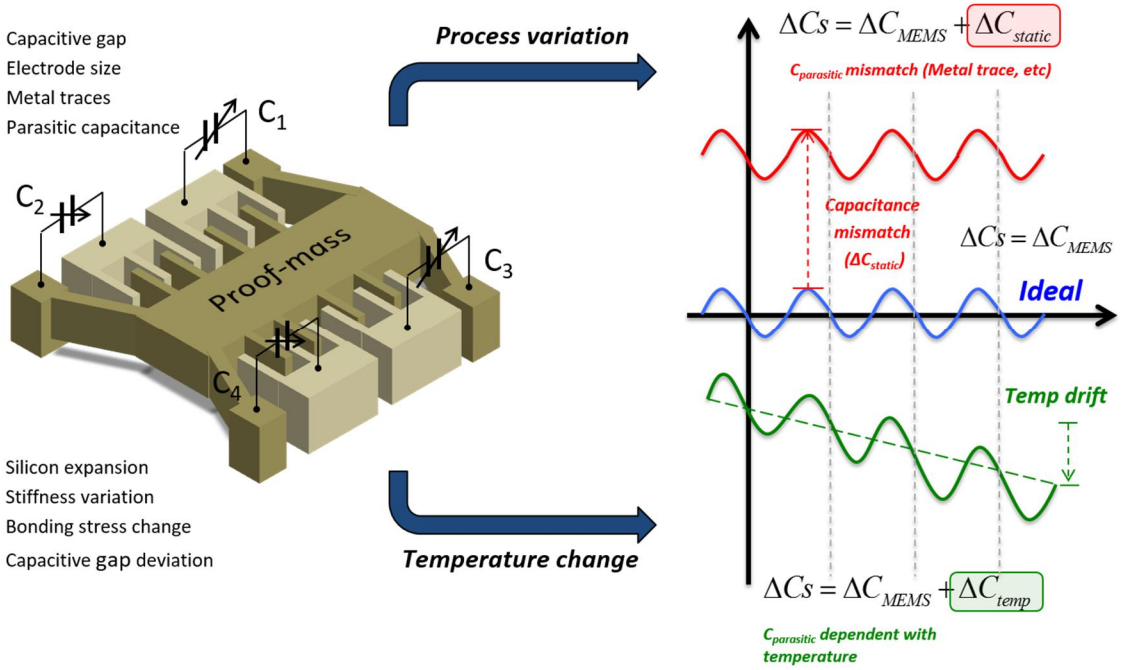


Figure 4. 16: Effect of environmental variation (capacitance mismatch or temperature change) on the accelerometer operation

The performance of MEMS sensor is extremely subject to the environmental conditions, such as parasitic capacitance mismatch or temperature change (Figure 4. 16). Such variations result in large offset or temperature-related drift that deteriorates the performance of the sensor. In this section, design and implementation of on-chip offset and temperature calibration block is presented.

4.3.1. Effect of Environmental Variation on MEMS Sensor

Actual capacitance distribution of the MEMS accelerometers was measured using Agilent E4980A Precision LCR meter as shown in Figure 4. 17 and Figure 4. 18. Although all the devices were fabricated on a same wafer using identical process, its standard deviation can be as high as 30 to 60 fF. If not handled properly, such mismatch can be a

serious issue, as it can be amplified into an offset level that is 6 to 8 times larger than actual output caused by the acceleration (Capacitive sensitivity: 5~10 fF/g).

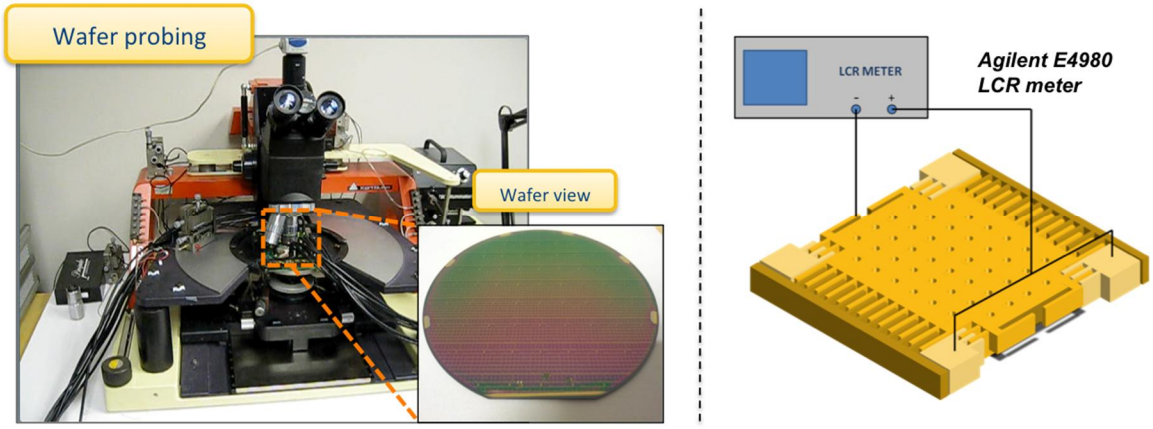


Figure 4. 17: (Left) Photo of wafer probing station (Right) Connection between LCR meter and MEMS accelerometer

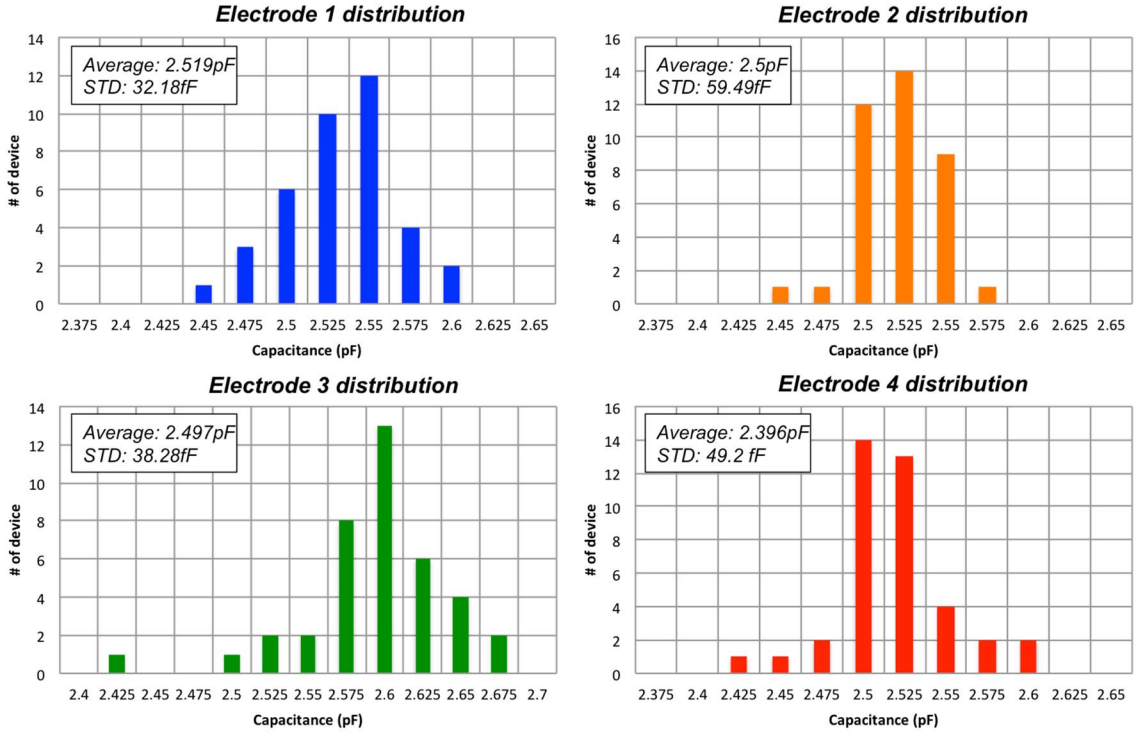


Figure 4. 18: Static capacitance distribution of 40 accelerometer devices

Commercial accelerometers have a separate target specification called *"Zero-acceleration bias level"*, which is the offset level of the output under stationary condition.

This parameter indicates the residual capacitive mismatch after the calibration of the interface circuit. Table 4. 2 summarizes the list of specifications on the zero-acceleration bias level that is used in commercial companies.

Table 4. 2: Zero-acceleration bias level specification for commercial accelerometers

Supplier	ST-micro (LIS3DH) [83]	Analog Device (ADXL345) [84]	Bosh (BMA250) [85]	Invensense (MPU6050) [86]
Zero-acceleration bias level	± 40 mg	± 150 mg	± 80 mg	± 80 mg

Change of ambient temperature level creates a thermal expansion or contraction on the microstructure, resulting in temperature dependent drift as expressed in equation (4-23), where α_L (Linear) or α_V (Volumetric) indicates the thermal expansion coefficient.

$$\Delta L = \alpha_L \cdot L \cdot \Delta T, \quad \Delta V = \alpha_V \cdot V \cdot \Delta T \qquad (4\text{-}23)$$

Thermal expansion coefficient (α_L) of the silicon (Si) is 2.8 ppm/°C [90], which leads to a change in length of 0.35 μm for a 100 μm long silicon beam when the temperature changes from -40 °C to 85 °C. Because of its miniscule geometry, such variation is large enough to significantly affect the sensor performance. Temperature variation becomes even more serious problem for a wafer-level-packaged (WLP) sensor, which uses eutectic or silicon fusion wafer bonding [91]. As the bonding materials (Copper, and Gold) has different thermal expansion coefficient, this creates a stress at the region of contact under different temperature level as shown in Figure 4. 19. Such behavior can tilt the proof-mass or affect the stiffness of mechanical spring, creating even larger and nonlinear temperature-dependent variation on MEMS sensor that is hard to calibrate.

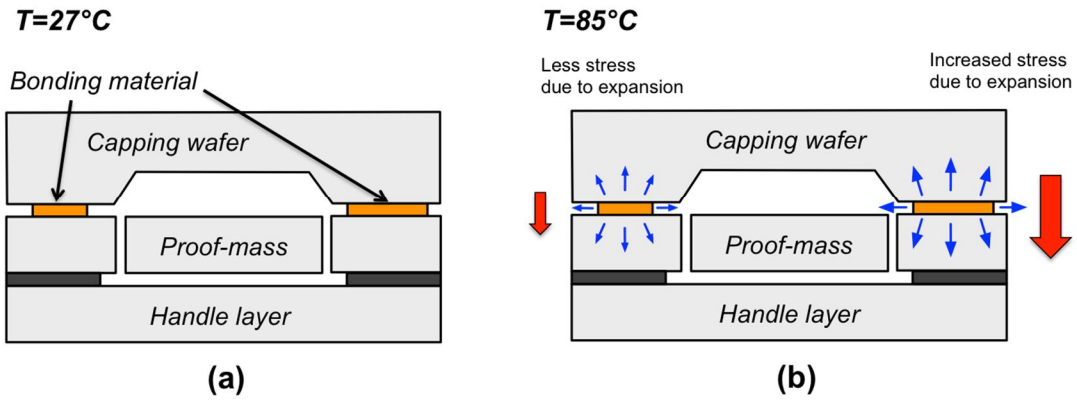


Figure 4. 19: Effect of the temperature variation on the wafer-level-packaged accelerometer

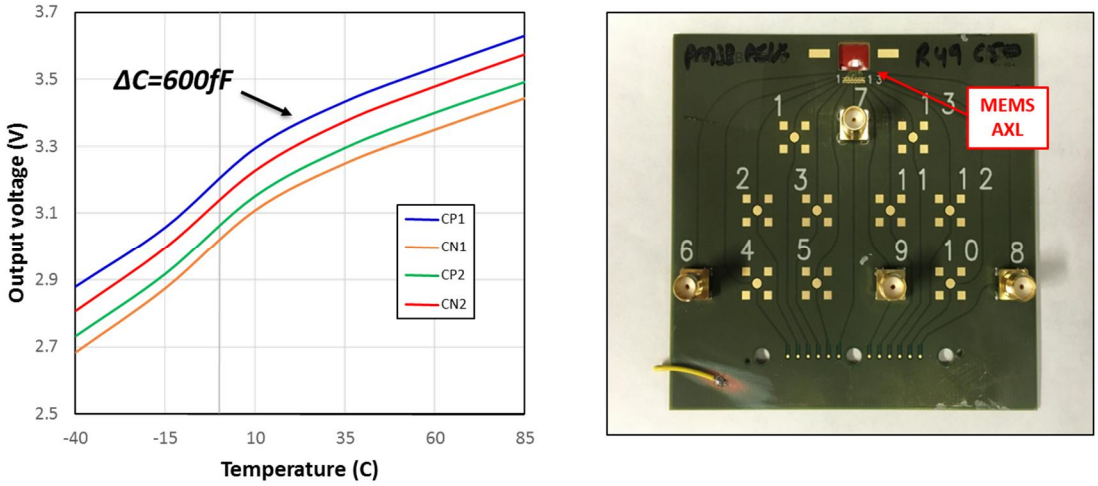


Figure 4. 20: (Left) Measured capacitance of MEMS accelerometer and (Right) Photo of evaluation board

Figure 4. 20 shows the measured capacitance of MEMS accelerometer under different temperature level. MEMS device was placed on top of custom-made evaluation board and inserted inside the chamber while sweeping the temperature from -40 °C to 85 °C. Result shows the overall capacitance variation can be as large as 600 fF, which is more than 50 times larger than the capacitive sensitivity of MEMS device. Commercial accelerometers also have specification for temperature stability, which is listed down as *"bias drift across the temperature"* in Table 4. 3. It indicates the change of bias level across the different temperature environment (-40 °C to 85 °C).

Table 4. 3: Temperature drift specification for commercial accelerometers

Supplier	ST-micro (LIS3DH) [83]	Analog Device (ADXL345) [84]	Bosh (BMA250) [85]	Invensense (MPU6050) [86]
Bias drift across temperature	± 0.5 mg/°C	± 0.4 mg/°C	± 1 mg/°C	± 0.85 mg/°C

4.3.2. TIME-AVERAGED CHARGE-TUNING OFFSET CALIBRATION

Table 4. 4 summarizes the target specification of the proposed offset calibration block. The target zero-acceleration bias level is set to ± 25 mg, which is a reasonable number considering the specifications from the commercial accelerometer (Table 4. 2). Assuming *"charge-tuning"* method [78] is used, to meet the required specification, resolution level for calibration voltage is equivalent to 0.781 mV when C_{OFFSET}=*200fF*.

$$V_{OUT} = \frac{0.5VDD}{C_F}\Delta C_{mismatch} + \frac{C_{offset}}{C_F}\Delta V_{CAL} \qquad (4\text{-}24)$$

Generating such fine voltage step size is a challenging task, as it increases the level of complexities and the required silicon areas for the calibration circuit. Although smaller offset capacitor *(e.g. 100 fF)* can be used to loosen the resolution specification, it would reduce the calibratable range by half.

Table 4. 4: Required target specification of offset calibration block

Performance parameter	**Target Value**
Zero-acceleration bias level	± 25 mg
Calibratable range	> 360 fF
Capacitive sensitivity of sensor	5 fF/g
Required resolution for calibration voltage to meet target resolution	0.39 mV @ C_{OFFSET}=400 fF, 0.781 mV @ C_{OFFSET}=200 fF 1.562 mV @ C_{OFFSET}=100 fF
Achievable calibration range	800 fF @ C_{OFFSET}=400 fF 400 fF @ C_{OFFSET}=200 fF 200 fF @ C_{OFFSET}=100 fF

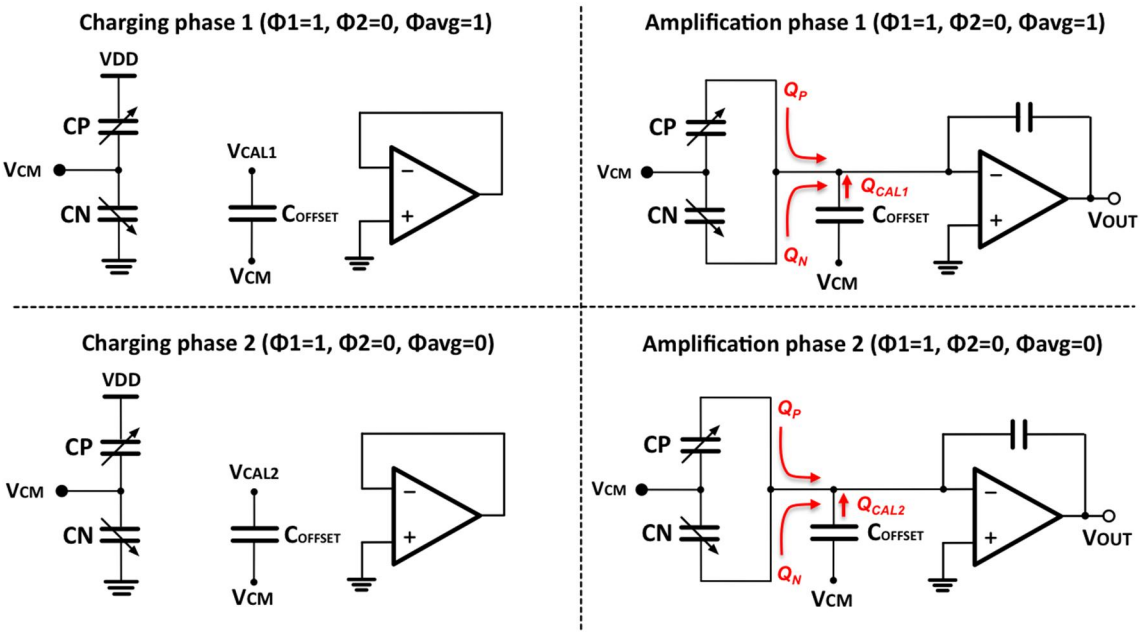


Figure 4. 21: Operation of SC-amplifier during time-averaging; Half circuit without CDS capacitor is shown for simplicity

To address the such issues, *"Time-averaging"* operation, which employs multiple calibration voltages that are controlled by the averaging clock phase *(Φ_{avg})*, is introduced as an extended feature of *"charge-tuning"* calibration. Whereas the *"charge-tuning"* method provides wide calibration range for the accelerometer, proposed *"time-averaging"* operation delivers a far precision control on the offset level. The basic operation is consisted of four separate phases as shown in Figure 4. 21. During its first charging phase *(Φ_1=1, Φ_2=0, Φ_{avg}=1)*, C_{OFFSET} is connected to calibration voltage V_{CAL1}, storing charge that is equivalent to equation (4-25). This charge is transferred to the SC-amplifier during consecutive amplification phase *(Φ_1=0, Φ_2=1, Φ_{avg}=1)*.

$$Q_{CAL1} = C_{OFFSET} \cdot (V_{CAL1} - V_{CMN}) \qquad (4\text{-}25)$$

On the second charging phase *(Φ_1=1, Φ_2=0, Φ_{avg}=0)*, C_{OFFSET} is tied to V_{CAL2}, which is one voltage step (i.e LSB) higher than the V_{CAL1}. Stored charge, which is

equivalent to equation (4-26) is also transferred to the SC-amplifier at second amplification phase *(Φ_1=0, Φ_2=1, Φ_{avg}=0)*.

$$Q_{CAL2} = C_{OFFSET} \cdot (V_{CAL2} - V_{CMN}) \qquad (4\text{-}26)$$

It is important to note that averaging clock is switching at much lower speed compared to the main clock *(Φ_{AVG}= Φ_1/16=Φ_2/16)* as shown in Figure 4. 22. The SC-amplifier output at the end of each amplification phase would have a different bias level depending on the averaging clock phase. That is, output would be equivalent to equation (4-27) when averaging clock is high *(Φ_{AVG}=1)* and equation (4-28) vice versa *(Φ_{AVG}=0)*.

$$V_{OUT1} = \frac{0.5VDD}{C_F}\Delta C_{accel} + \frac{C_{OFFSET}}{C_F}(V_{CAL1} - V_{CMN}) \qquad (4\text{-}27)$$

$$V_{OUT2} = \frac{0.5VDD}{C_F}\Delta C_{accel} + \frac{C_{OFFSET}}{C_F}(V_{CAL2} - V_{CMN}) \qquad (4\text{-}28)$$

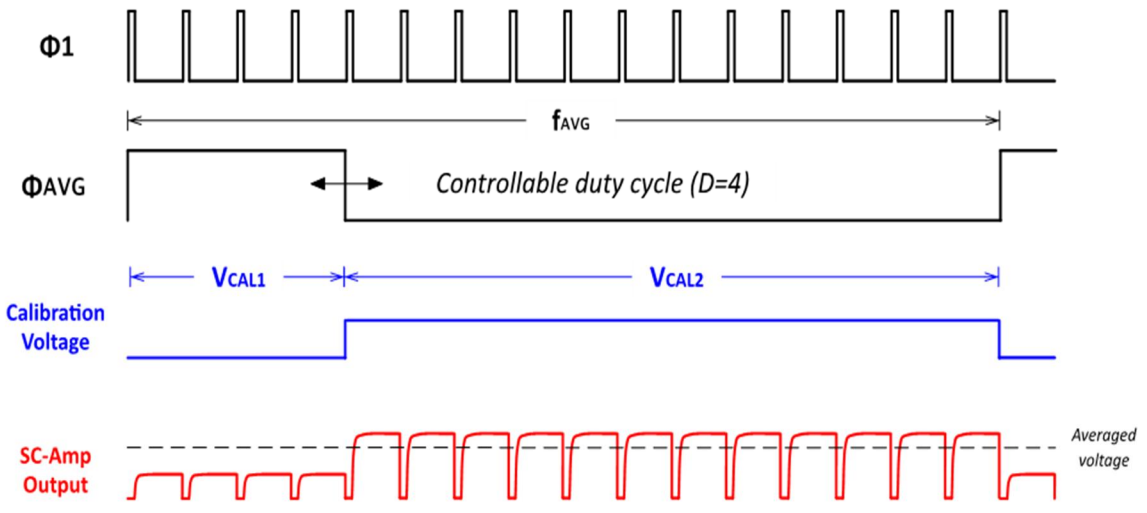


Figure 4. 22: Clock phase diagram and SC-amplifier output during time-averaging operation

There will be ripples at the SC-amplifier output due to switching between different voltage levels *(V_{OUT1} & V_{OUT2})*. But these signals are relatively small and switches (*f_{avg}=46.875 kHz)* far beyond the resonance bandwidth of the accelerometer *(f_{res}≈15 kHz*). Therefore, such signals can be easily filtered out, which leaves only the averaged output between V_{OUT1} and V_{OUT2}. This is determined by the duration of each calibration signals *(t_{CAL1} & t_{CAL2})* within the averaging clock period *(t_{period})* as expressed in equation (4-29).

$$V_{OUT.AVG} = \frac{0.5VDD}{C_F}\Delta C_{accel} + \frac{C_{offset}}{C_F}\left[\frac{t_{CAL1}}{t_{period}}(V_{CAL1} - V_{CMN}) + \frac{t_{CAL2}}{t_{period}}(V_{CAL1} - V_{CMN})\right] \qquad (4\text{-}29)$$

The main concept of the *"time-averaging"* is to change the duty cycle of the averaging clock *(Φ_{AVG})* to tune the bias level in fine step size. As the duty cycle control is done using digital blocks, improved resolution can be achieved and the operation is less susceptible to temperature or process variation.

Schematic diagram of the overall offset calibration circuit, which is consisted of calibration voltage generator, switching core, and duty cycle controller, is shown on Figure 4. 23. The calibration voltages, V_{CAL1} and V_{CAL2} are generated from the resistor ladder, implemented by the two sets of 8-bit binary weighted resistors R_1 and R_3 (equation (4-30)). Resistor R_2 is equivalent to minimum resistance that is used inside the binary weighted resistors, so that there will be 1 LSB difference (=10 mV) between V_{CAL1} and V_{CAL2}. The calibration voltage can be swept from 0 to 2.5 V within 10 mV step.

$$V_{CAL1} = VDD \cdot \frac{R_3}{R_1 + R_2 + R_3}, \quad V_{CAL2} = VDD \cdot \frac{R_2 + R_3}{R_1 + R_2 + R_3} \qquad (4\text{-}30)$$

The input of the switching core is gated with two set of switches controlled by the averaging clock *(Φ_{AVG})*. When the *"time-averaging"* function is enabled, these switches are constantly toggled to feed the switching core with either of two voltages, V_{CAL1}, and V_{CAL2} and charge the offset capacitor C_{offset}. The default C_{offset} is 200 fF, which guarantees calibration range closed to 400 fF. This range can be increased to 1.6 pF by enabling *Range* switch, which boosts the C_{offset} into 800 fF. Of course, as the step size of calibration voltage remains constant, its resolution level will be degraded by four times.

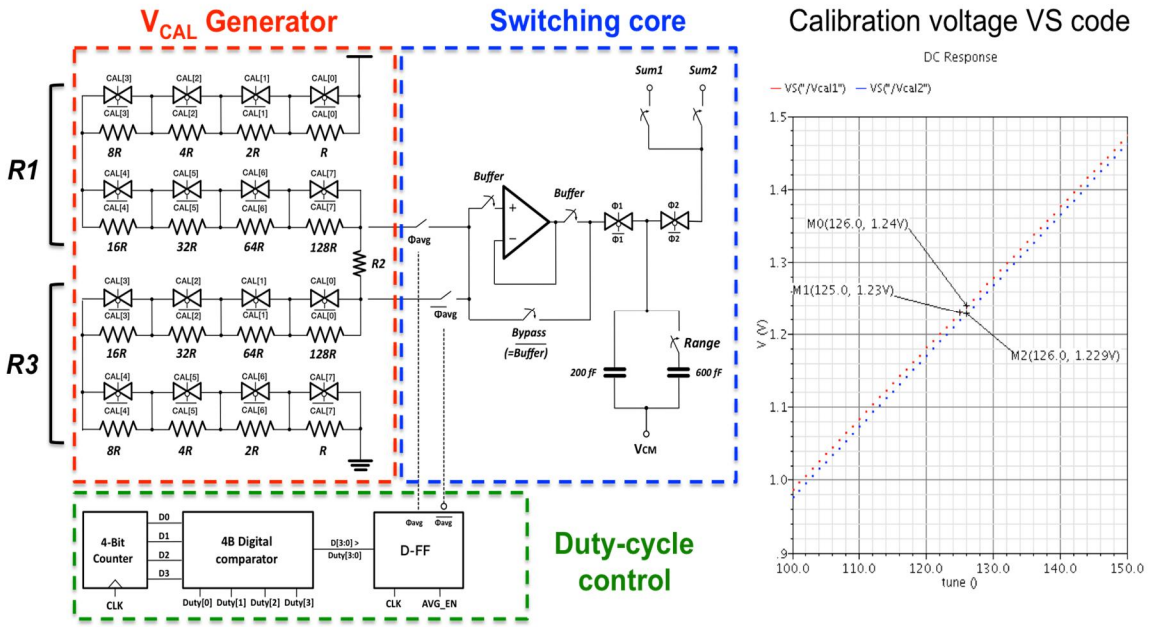


Figure 4. 23: (Left) Schematic of on-chip offset calibration block and (Right) simulation of calibration voltage with respect to register setting

The duty cycle controller is implemented by combining 4-bit counter and digital comparator as shown in Figure 4. 24(a). When the counter counts the number from 0 to 15, digital comparator, which constantly monitors between counted number and predefined 4-bit threshold settings *(Duty[3:0])*, generates 1 *(C[3:0]< Duty[3:0])* or 0 *(C[3:0]≥ Duty [3:0])*. This operation creates an averaging clock signal, which duty cycle can be adjusted

based on given threshold bit. The simulation results at Figure 4. 24(b) show the duty cycle of averaging clock changes with given settings.

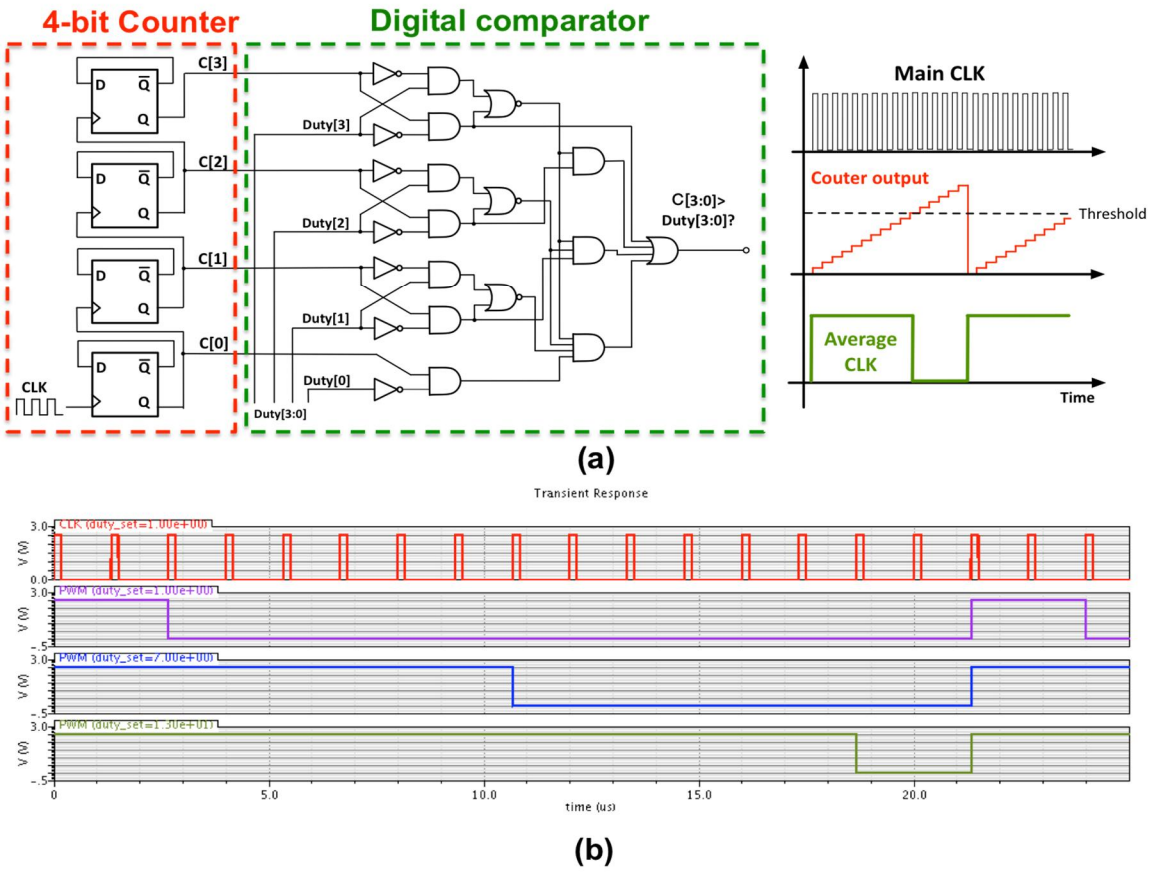


Figure 4. 24: (a) Schematic diagram and (b) transient simulation result of duty-cycle control circuit under different configuration

Figure 4. 25(a) shows the simulated SC-amplifier output with respect to different calibration voltage settings *(Offset[7:0])*. The *"time-averaging"* function is disabled to solely characterize the performance of *"charge-based"* calibration. When the circuit gain is 2.93 mV/fF, the output level changes from -0.7 V to 0.7 V, which corresponds to calibration range of 477 fF. Figure 4. 25(b) shows the changes in output level with respect to different duty-cycle when *"time-averaging"* is enabled. The averaged step size between each setting is 1.5 mV, which corresponds to capacitive resolution of 127 aF considering

the circuit gain is 11.72 mV/fF. Assuming the scale factor of sensor is 5 fF/g, measured capacitive resolution is translated into *"zero-acceleration bias level"* of 25.4 mg.

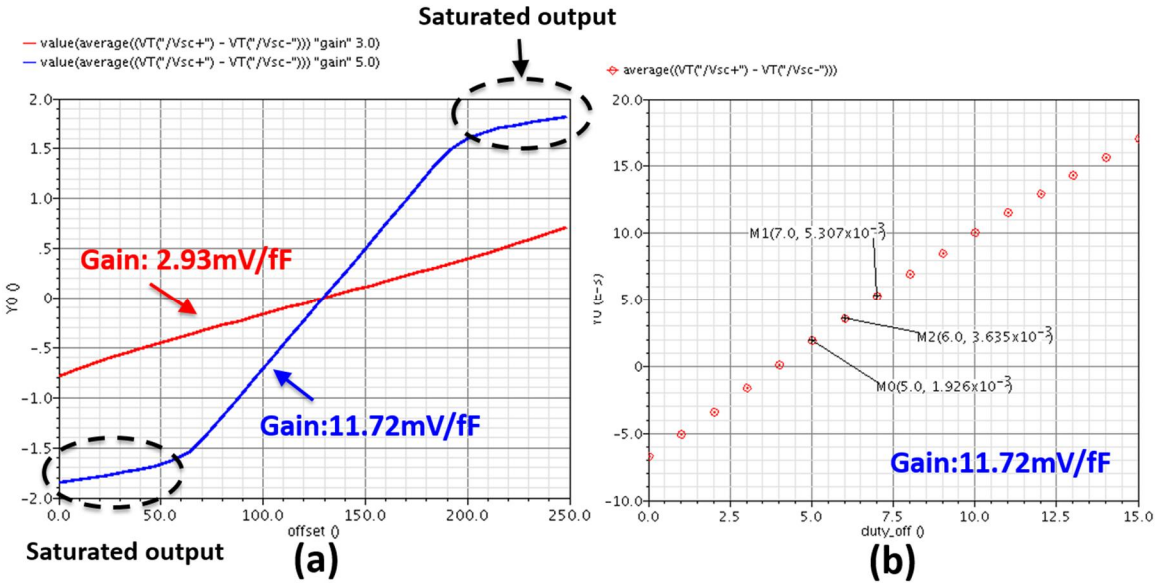


Figure 4. 25: Simulated SC-amplifier output with different (a) calibration voltage and (b) the duty-cycle settings

4.3.3. TEMPERATURE COMPENSATION BLOCK

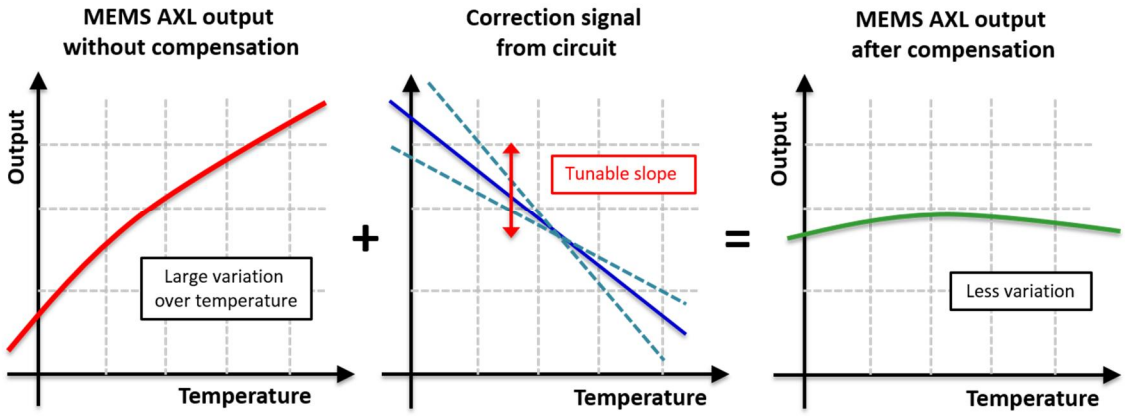


Figure 4. 26: System diagram showing temperature compensation process

Temperature dependent variation on MEMS accelerometer output is suppressed by adding a correction signal, which has a programmable slope (i.e. temperature coefficient (TC) as shown in Figure 4. 26. The final compensated output would have a minimum

variation over the temperature by giving right TC setting. The temperature compensation block needs to have fine slope trimming capability as well as wide calibration range, so that the residual variation does not exceed the target specification shown in Table 4. 5.

Table 4. 5: Required target specification of temperature compensation block

Performance parameter	Target Value
Bias drift across temperature	± 0.5 mg/ ºC
Temperature compensation range	> 6 g
Capacitive sensitivity of sensor	5 fF/g

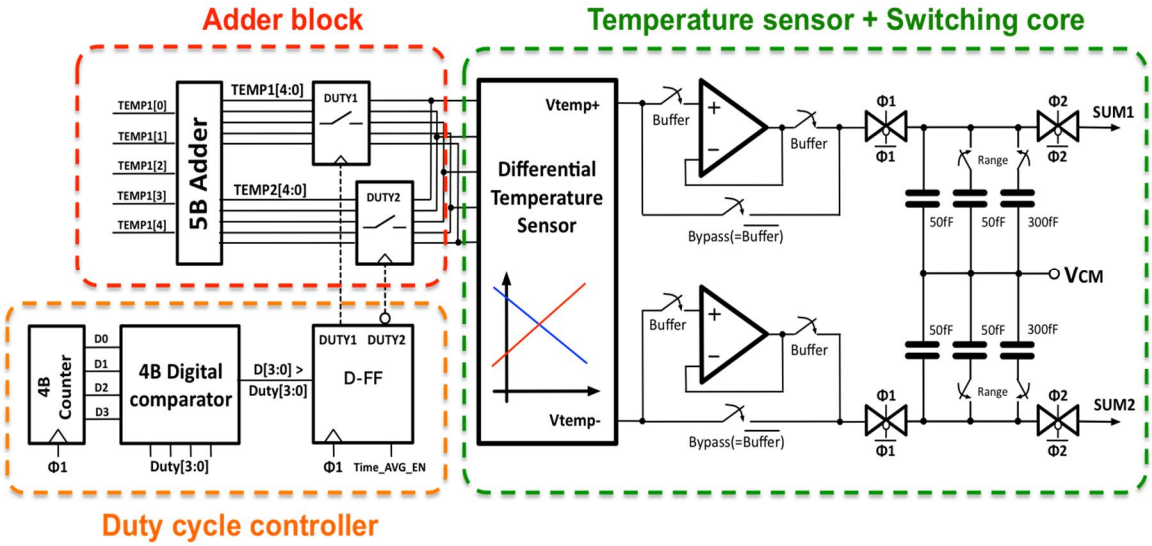


Figure 4. 27: Schematic diagram of the temperature compensation block using time-averaging method

Temperature compensation block uses similar methodology as in offset calibration (Figure 4. 23). Only difference is the replacement of calibration voltage generator with the temperature sensing circuit. The overall schematic diagram in Figure 4. 27 shows the proposed compensation block, which is consisted of differential temperature sensor, switching core, adder block, and duty-cycle controller. During operation, temperature sensor consecutively changes capacitor C_{temp} with differential voltages $(V_{temp+}$ & $V_{temp-})$,

transferring compensation charges into SC-amplifier through its summing nodes *(Sum1 & Sum2)*. Usig the law of charge conservation, the resulting output of SC-amplifier can be derived as equation (4-31), where ΔC_{accel} represents the change of capacitance due to applied acceleration, and ΔC_{temp} as the non-ideal capacitance change due to temperature. Amount of change between V_{temp+} and V_{temp-} with respect to ambient temperature level is programmable using 5-bit register setting in temperature sensing circuit. By trimming its slope, non-ideal bias drift of the accelerometer can be minimized.

$$V_{OUT} = \frac{0.5VDD}{C_F}\left(\Delta C_{accel} + \Delta C_{temp}\right) + \frac{C_{temp}}{C_F}\left(V_{temp+} - V_{temp-}\right) \qquad (4\text{-}31)$$

The compensation block also incorporates the *"Time-averaging"* method to attain finer resolution level between each TC configuration. When enabled, two different settings $TEMP_1[4:0]$ and $TEMP_2[4:0]$, which is 1 LSB apart, are applied to temperature sensor to control its the output slope. Similar to offset calibration, the average clock (Φ_{AVG}) phase determines which setting will be used to set the TC of the temperature sensor.

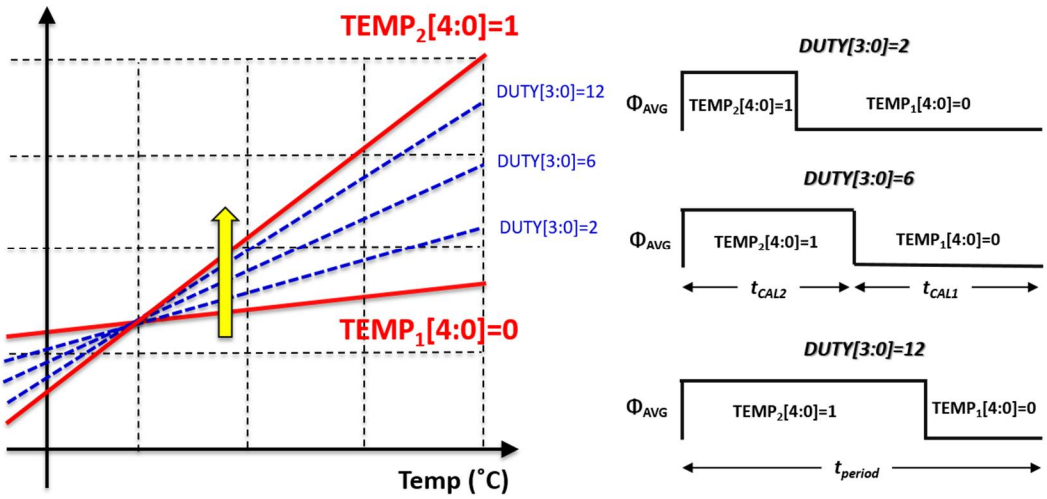


Figure 4. 28: Diagram showing behavior of compensation signal with respect to ambient temperature on different slope setting

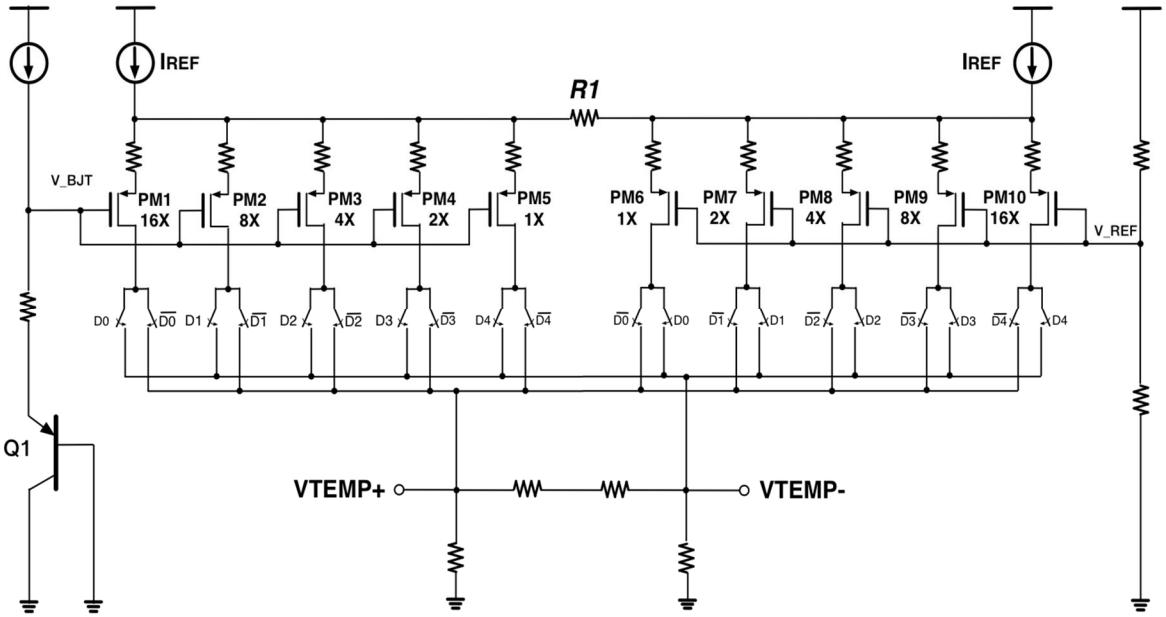


Figure 4. 29: Schematic of temperature sensor used in compensation block

As the averaging clock is switching at far higher speed than the operational bandwidth of accelerometer, only the averaged TC between two settings remains at final output. Similar to offset calibration block, by changing the duty cycle of the average clock *(Φ_{AVG})*, the resulting slope can be trimmed in much finer scale as shown in Figure 4. 28. Transfer function of the temperature compensation block with *"time-averaging"* is expressed in equation (4-32). ΔV_{temp1} represents the differential voltage (V_{temp+} - V_{temp-}) of the temperature sensor when the TC setting is equivalent to $TEMP_1$[4:0] and ΔV_{temp2} when $TEMP_2$[4:0]. t_{CAL1} and t_{CAL2} is the duration of time when each slope setting is enabled during t_{period}.

$$V_{OUT} = \frac{0.5VDD}{C_F}\Delta C_{accel} + \frac{C_{temp}}{C_F}\left[\frac{t_{CAL1}}{t_{period}}\Delta V_{temp1} + \frac{t_{CAL2}}{t_{period}}\Delta V_{temp2}\right] \qquad (4\text{-}32)$$

The schematic of the differential temperature sensor is shown in Figure 4. 29. It is consisted of binary weighted current sourcing transistors *PM1 ~ PM10* to create 5-bit

programmability on its temperature coefficient (TC). BJT transistor Q_1 generates a base-emitter voltage, which have *CTAT (Complementary to Absolute Temperature)* characteristic as shown in equation (4-33), where E_g is the bandgap voltage of the semiconductor, q is the electron charge respectively.

$$\frac{\partial V_{BE}}{\partial T} = \frac{V_{BE0} - (4+m)V_T - E_g/q}{T} \qquad (4\text{-}33)$$

This voltage is connected to the gate of current sourcing transistors *PM1 ~ PM5*. As each gate is binary weighted sized, the induced current can be expressed as equation (4-34) to (4-35), where α represents the TC and β as the Y-intercept.

$$I_{PM1} = 16 \cdot (\alpha T + \beta),\ I_{PM2} = 8 \cdot (\alpha T + \beta),\ I_{PM3} = 4 \cdot (\alpha T + \beta) \qquad (4\text{-}34)$$

$$I_{PM4} = 2 \cdot (\alpha T + \beta),\ I_{PM5} = 1 \cdot (\alpha T + \beta) \qquad (4\text{-}35)$$

Transistor *PM6 ~ PM10* induces another set of current with opposite polarity as shown in equation (4-36) and (4-37). This is caused by the resistor R_1, which connects the two groups of binary weighted transistor, and let the current to flow between each other.

$$I_{PM6} = 1 \cdot (-\alpha T + \beta),\ I_{PM7} = 2 \cdot (-\alpha T + \beta),\ I_{PM8} = 4 \cdot (-\alpha T + \beta) \qquad (4\text{-}36)$$

$$I_{PM9} = 8 \cdot (-\alpha T + \beta),\ I_{PM10} = 16 \cdot (-\alpha T + \beta) \qquad (4\text{-}37)$$

SPDT (Single-Pole Double-Throw) switches are placed after the current sourcing transistors *PM1~PM10* to provide programmable TC at the differential output. Depending on which side of the switch is closed, induced currents are rerouted into either of positive (V_{TEMP+}) or negative (V_{TEMP-}) output, generating an output voltage with different

temperature dependent slope. Figure 4. 30(a) shows the simulated temperature sensor output with respect to ambient temperature level from -40 ºC to 85 ºC. The output slope changes its value depending on the applied TC setting. Calculated slopes are plotted with different setting on Figure 4. 30(b), where the TC sweeps from -5.15 mV/ ºC to 5.15 mV/ ºC with 0.3 mV/ ºC step size.

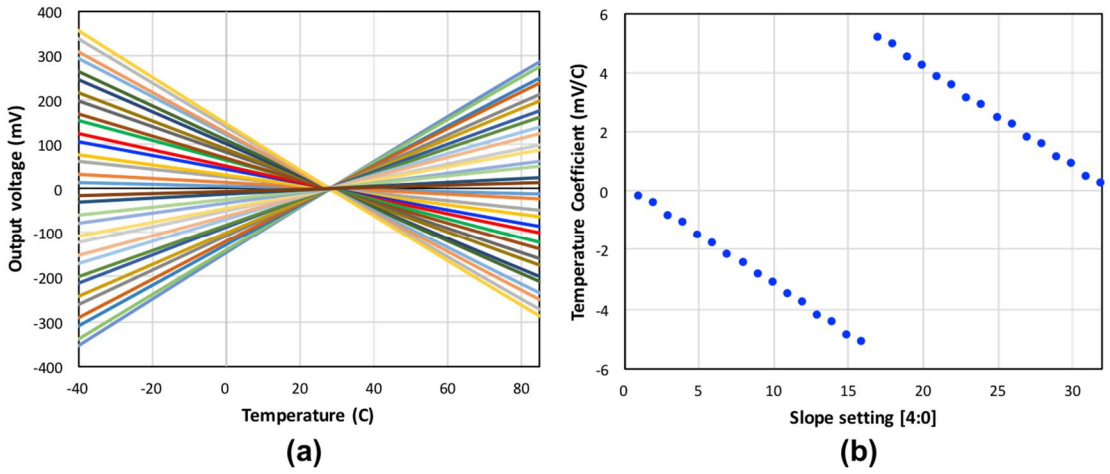
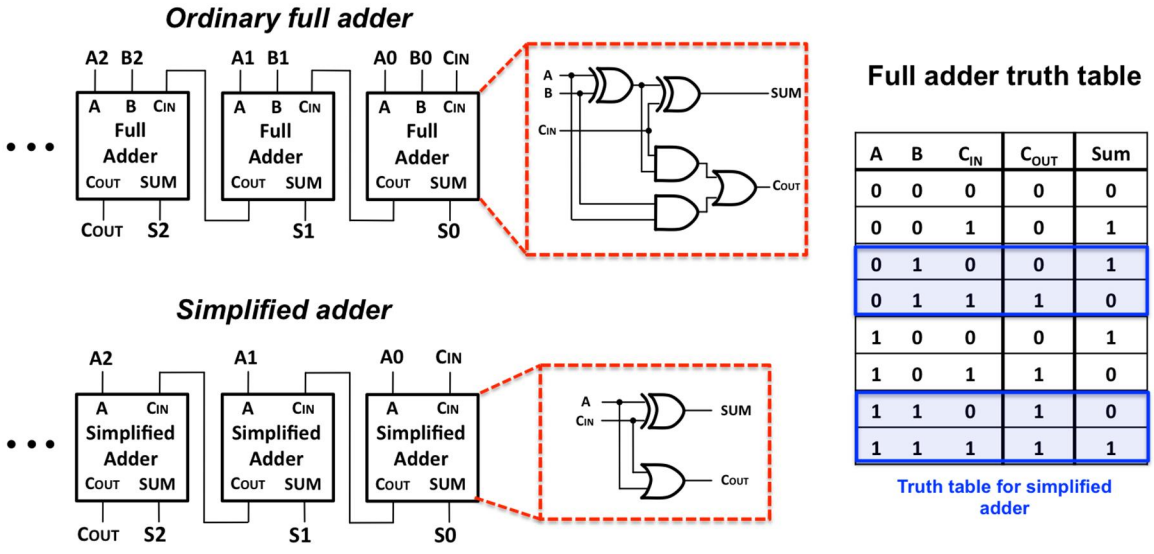


Figure 4. 30: (a) Simulation result of temperature sensor output under different temperature level and (b) its temperature coefficient (TC) with respect to slope setting



A	B	C_{IN}	C_{OUT}	Sum
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

Figure 4. 31: Schematic diagram of simplified adder compared with ordinary full adder

Adder block shown in Figure 4. 27 and Figure 4. 31 generates two different TC settings $TEMP_1$[4:0] and $TEMP_2$[4:0] for *"time-averaging"* function. The schematic of adder block is shown on Figure 4. 31. As the purpose of the adder block is to create different codes by adding 1-bit to input register, simplified version was implemented rather than using ordinary full-adder architecture.

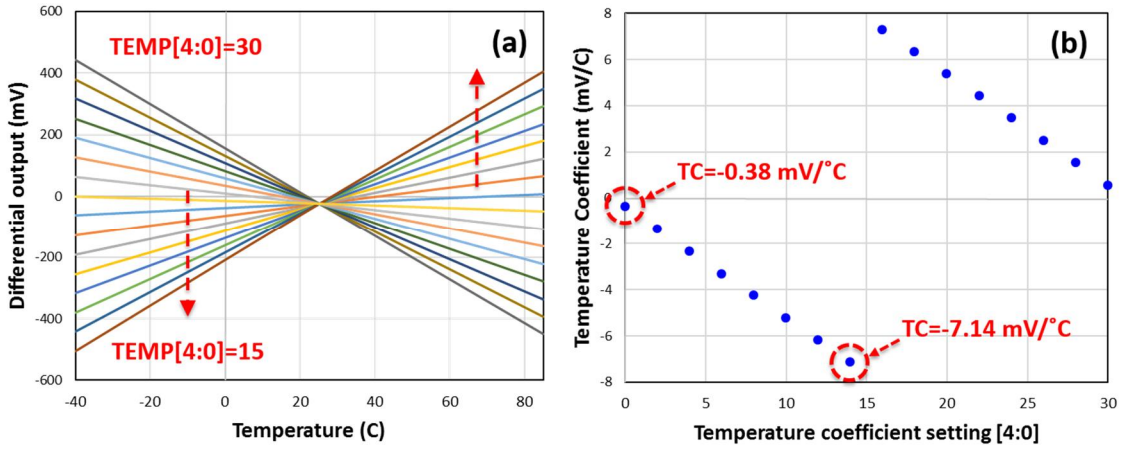


Figure 4. 32: Simulation result of SC-amplifier with temperature compensation (Disabling time-averaging function)

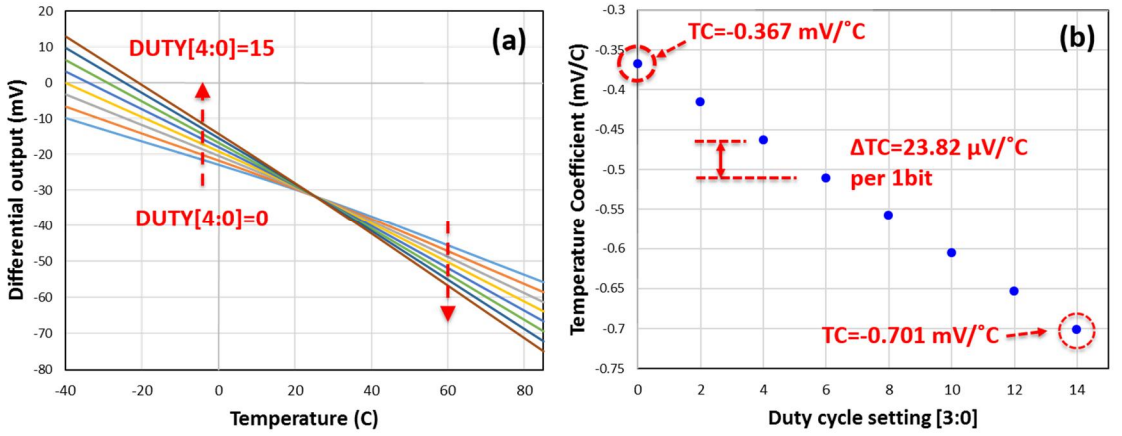


Figure 4. 33: Simulation result of SC-amplifier with temperature compensation (Enabling time-averaging function)

Simulation result of temperature compensation block is shown in Figure 4. 32 and Figure 4. 33. When the "time-averaging" operation is disabled, the temperature dependent

slope of the SC-amplifier changes by 0.481 mV/ºC per bit from -7.13 mV/ºC to 7.29 mV/ºC. When "time-averaging" is enabled, the output slope changes by 23.82 µV/ºC per 1 duty cycle. Assuming capacitive sensitivity of MEMS sensor + ASIC is 78.125 mV/g, this is equivalent to 0.305 mg/ºC.

4.3.4. SIGMA-DELTA MODULATOR DESIGN

Generated current from the G_m-cell is converted into digital domain using ΣΔ modulation. Although there are various analog-to-digital conversion techniques, ΣΔ modulation is best suit for inertial sensor application, for its exceptional noise-shaping characteristic that up-converts the quantization noise within the low-frequency operational bandwidth.

The simplified diagram of first order ΣΔ modulator is shown on Figure 4. 34(a), which is consisted of integrator and 1-bit quantizer. Its purpose is to read incoming signal and convert it into 1-bit pulse density stream and hand it over to decimation filter. To analyze the noise-shaping property, the overall block is simplified as Figure 4. 34(b). The 1-bit quantizer is represented as an additive noise source.

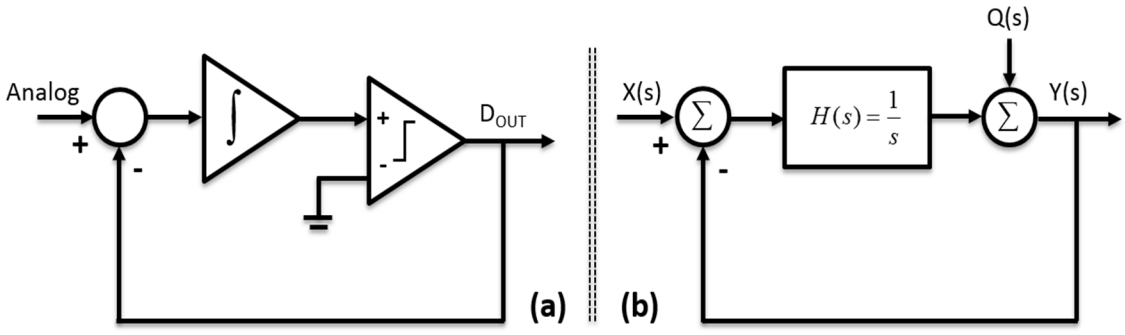


Figure 4. 34: (a) Block diagram and (b) simplified signal flow diagram of 1st order ΣΔ modulator

The signal transfer function (STF) and the noise transfer function (NTF) of the ΣΔ modulator can be derived as equation (4-38) and (4-39).

$$STF = \frac{Y(s)}{X(s)} = \frac{H(s)}{1+H(s)} = \frac{1}{1+s} \qquad (4\text{-}38)$$

$$NTF = \frac{Y(s)}{Q(s)} = \frac{1}{1+H(s)} = \frac{s}{1+s} \qquad (4\text{-}39)$$

As can be seen from the equation, the STF follows a low-pass filter characteristic whereas the NTF shows band-reject behavior at the DC level so that the quantization noise can be up-converted into higher frequency. This property is called the noise-shaping, and its DC rejection gets even steeper as the number of order gets higher as Figure 4. 35.

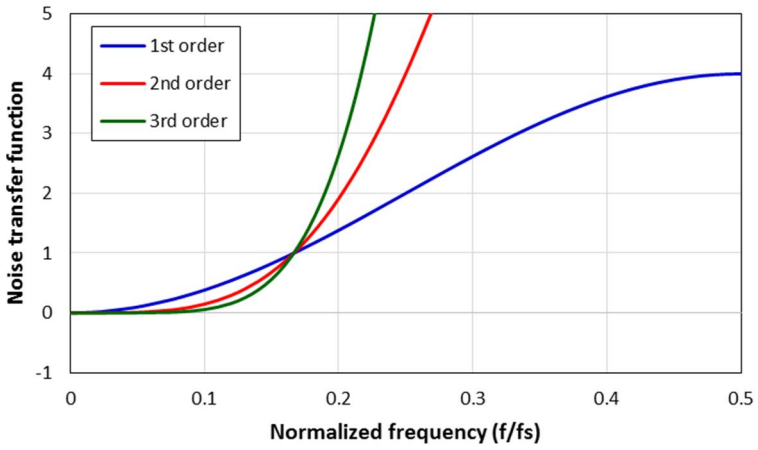


Figure 4. 35: Noise transfer function (NTF) of ΣΔ modulator under different order

Proposed accelerometer circuit employs 3rd order continuous-time ΣΔ architecture with distributed feedback (Figure 4. 36) for its advantage on low-power consumption and not needing of separate anti-aliasing filter. G_m-C approach was used to implement integrators as it has wider bandwidth and low-power consumption compared to other active-filter method. Furthermore, the G_m-cell block located after the SC-amplifier can be

utilized to construct 1st integrator as well, which will save required silicon area and complexity. All of the integrator has programmable current (I_{DAC}) and capacitor ($C_1/C_2/C_3$) to trim its value so that optimum transfer function can be achieved. Generated bit-stream from modulator goes into the decimation filter, which removes the up-converted quantized noise, and demultiplex incoming signal into three separate channels (*x/y/z*- axis).

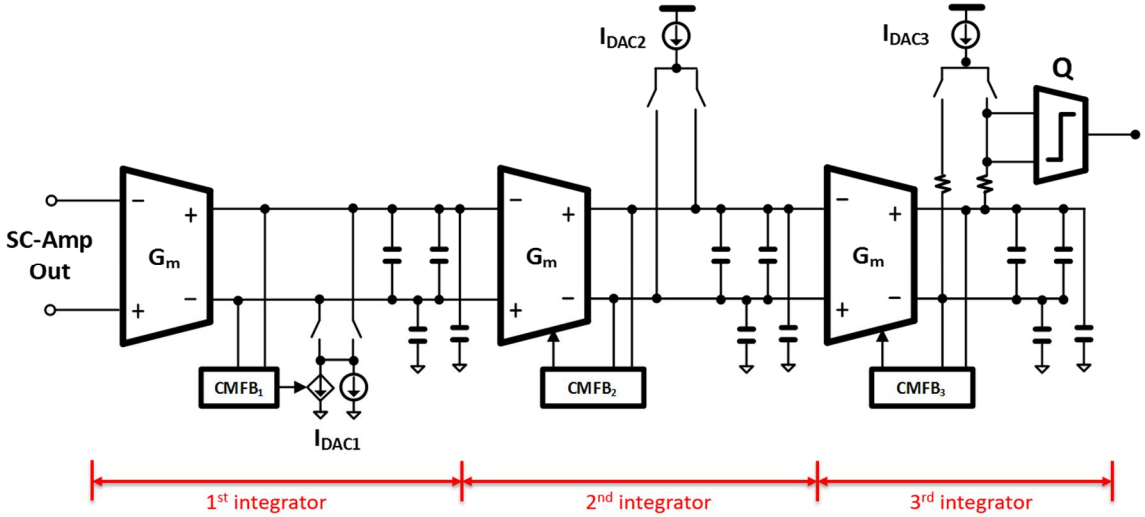


Figure 4. 36: Schematic diagram of ΣΔ modulator

4.4. Measurement Result

4.4.1. ASIC-Only Configuration

Before interfacing with the sensor element, the configuration of the circuit was set to "ASIC-only", which connects the on-chip MIM (Metal-Insulator-Metal) capacitor to the input of SC-amplifier instead (Figure 4. 37). Doing so helps characterizing the performance of the sole circuit without being affected by any non-ideal behavior from MEMS device. Initial functionality was verified by probing multiple nodes inside the interface circuit

using calibration buffer (Figure 4. 38). The output waveform clearly shows the charging *(Φ_1=1, Φ_2=0)* and amplification phase *(Φ_1=0, Φ_2=1)* of the SC-amplifier.

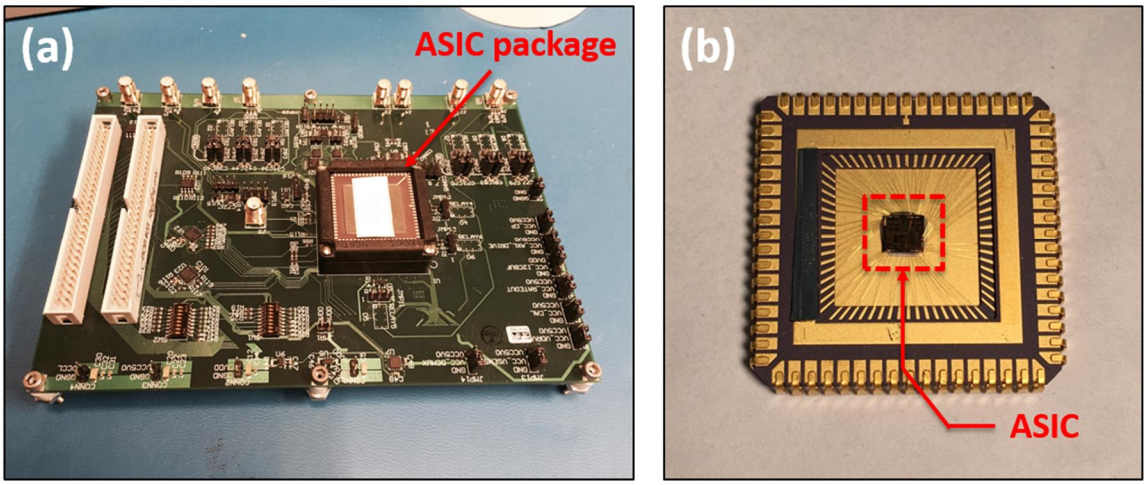


Figure 4. 37: Photo of (a) evaluation board and (b) interface ASIC bonded to ceramic package

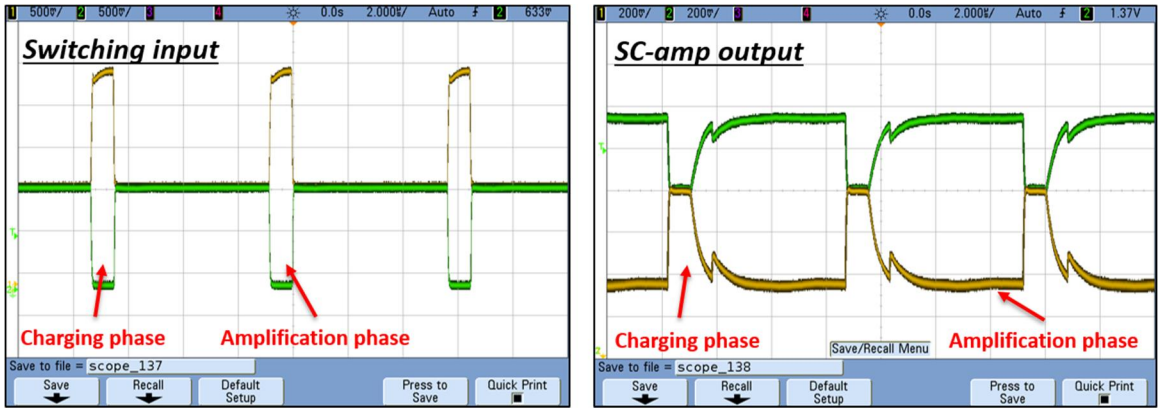


Figure 4. 38: Output waveform of calibration buffer while probing multiple nodes inside the SC amplifier

The cancellation of capacitive mismatch was verified by observing the SC-amplifier output while sweeping the calibration voltage from 0 to 2.5 V as shown in Figure 4. 39. Measurement result shows the calibration circuit can achieve average resolution level of 1.22 fF while maintaining full calibration range of 374 fF. When “time-averaging” is enabled and the duty-cycle setting was changed as shown in Figure 4. 39 (b), the average

resolution level drops down to 71.76 aF. Assuming sensor sensitivity is 5 fF/g, this is equivalent to 14.35 mg, which satisfies the target specifications.

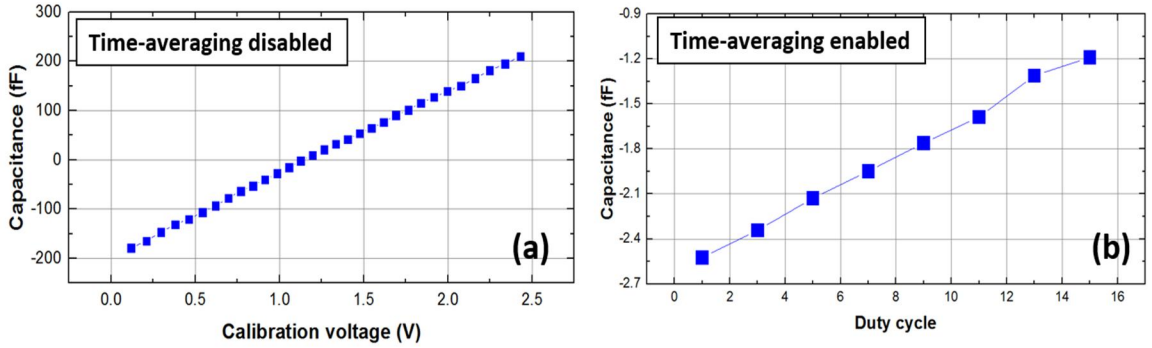


Figure 4. 39: Measured capacitance mismatch of SC-amplifier (ASIC-only) with respect to different calibration setting when (a) time-averaging is disabled and (b) enabled

Figure 4. 40 shows the measured output of the temperature sensor and SC-amplifier from -40ºC~85ºC under different temperature coefficient (TC) setting (ASIC-only). The graph shows the TC of SC-amplifier can be trimmed from -4.64mV/°C to 4.32 mV/°C. This shows the temperature compensation block can suppress capacitance variation of MEMS accelerometer up to -7.42 g from 6.91 g over entire temperature range (Assuming nominal sensitivity of MEMS+ASIC=78.1 mV/g).

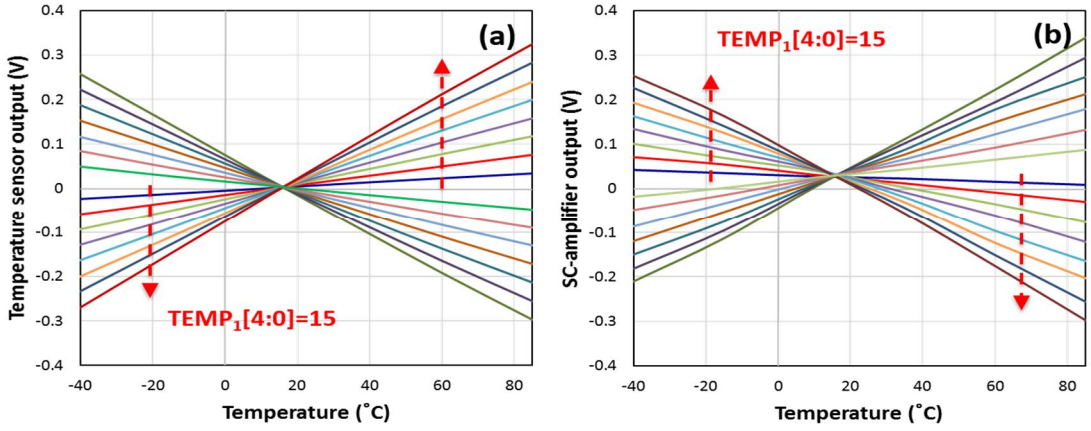


Figure 4. 40: Measured differential output from (a) temperature sensor and (b) SC-amplifier under different TC setting when time-averaging is disabled

When the time-averaging function is enabled, the TC of the SC-amplifier changes in much finer scale as shown in Figure 4. 41. Measurement shows the average step size between each TC value is approximately 27.7 µV/°C. This is equivalent to 0.354 mg/°C of residual drift on MEMS accelerometer after temperature compensation process.

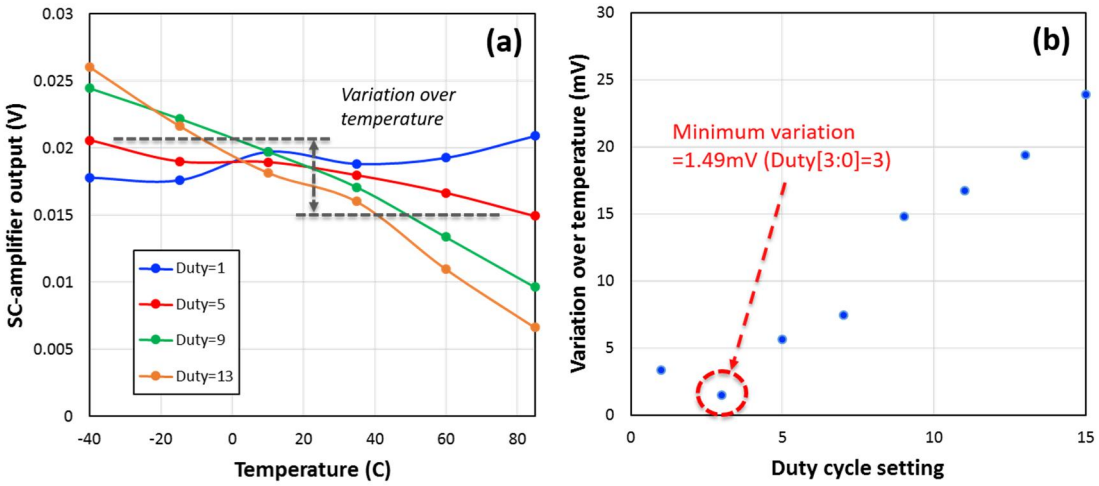


Figure 4. 41: Measured (a) differential output from SC-amplifier and (b) overall variation over temperature under different TC setting when time-averaging is enabled.

4.4.2. ASIC+MEMS CONFIGURATION

MEMS accelerometers were interfaced with presented low-noise low-offset readout circuit as shown in Figure 4. 42 and its overall system performance was characterized. As a first step, the inherent capacitive mismatch on MEMS sensor was suppressed by means of on-chip calibration circuit. The offset level of multiple devices (27 in-plane and 18 out-of-plane accelerometers) were calibrated to get the statistical distribution data. As shown in Figure 4. 43, before calibration process, the standard deviation of capacitance mismatch was 55. 92 fF and 387.82 fF for each in-plane and out-of-plane design respectively. Larger C_{OFFSET} value was used during calibration of out-of-

plane accelerometer to account for its large capacitive mismatch compared to in-plane design. After the correction process, the mismatch levels mismatches are suppressed drastically down to 77.94 aF and 156.66aF, which is equivalent to 57.12 dB and 67.87 dB. This is more than 10 dB improvement compared to other state-of-art calibration circuit that was reported earlier [76] [77].

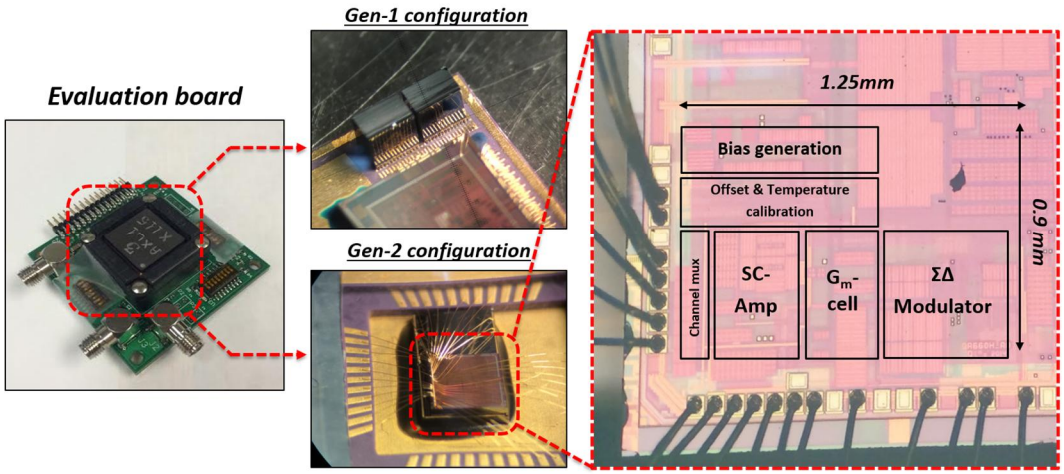


Figure 4. 42: Microphotograph of WLP accelerometer (*Gen-1* & *Gen-2*) interfaced with readout circuit and closed-up view on ASIC

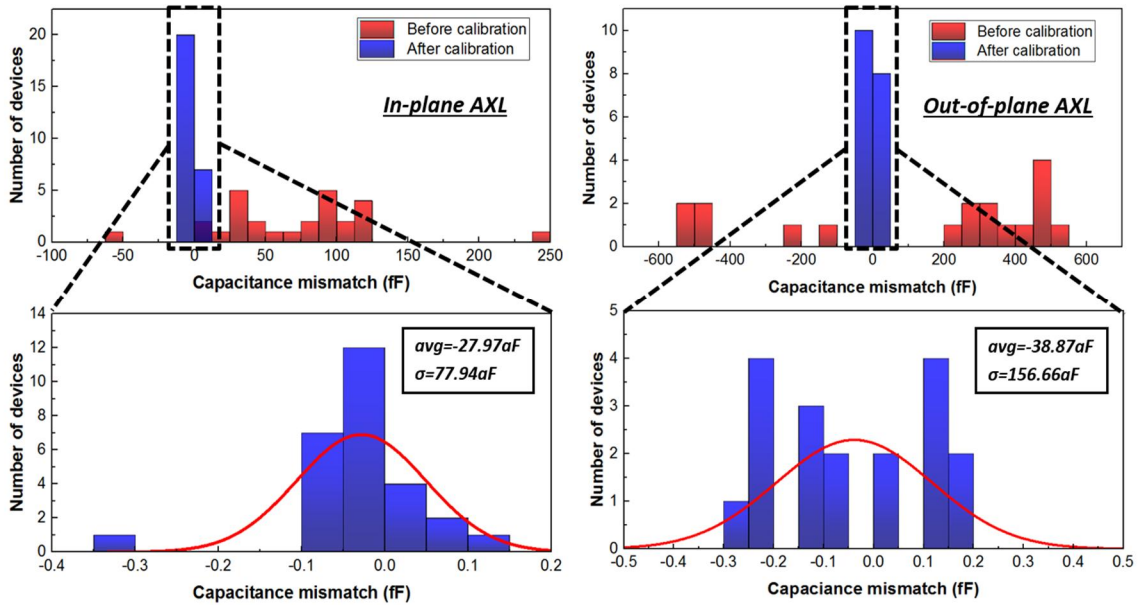


Figure 4. 43: Statistical distribution of capacitance mismatch on in-plane and out-of-plane MEMS accelerometer while enabling and disabling offset calibration

The scale factor of the MEMS accelerometer was measured by applying acceleration into *x-/y-/z-* axis directions using ET-126 shaker table as shown in Figure 4. 44. Its transient response under 1g acceleration is plotted at Figure 4. 45 and Figure 4. 45. At maximum gain setting, analog output of the *Gen-1* accelerometer shows differential sensitivity of 163 mV/g,.

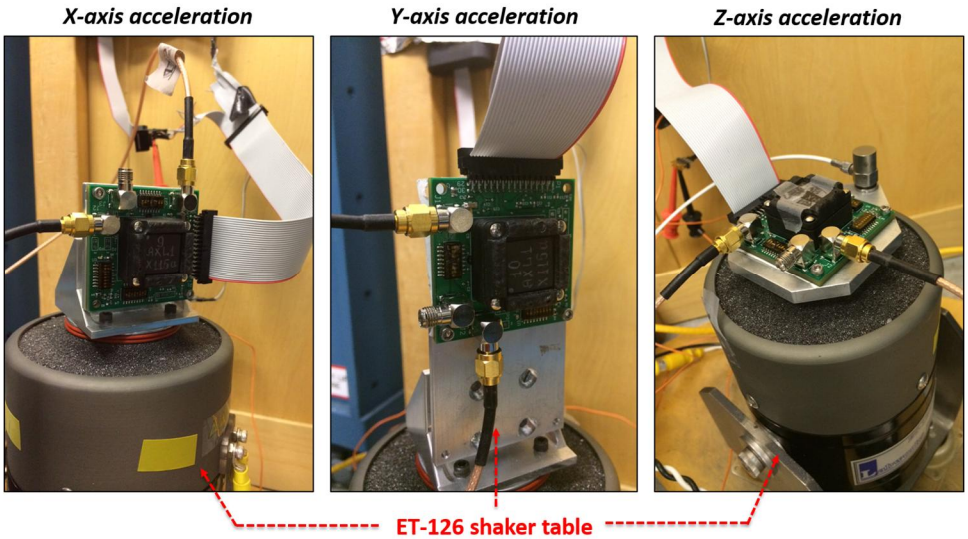


Figure 4. 44: Photo of evaluation board attached to shaker table under different axes of acceleration

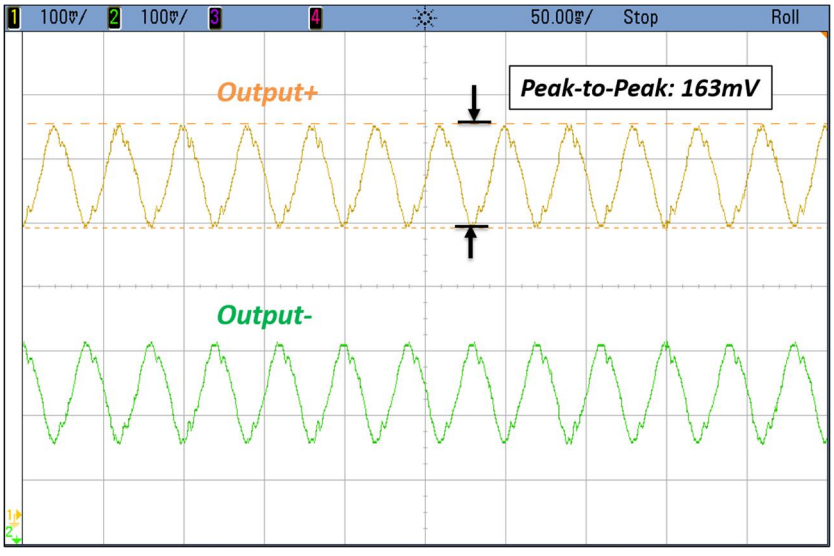


Figure 4. 45: Measured analog output from the *Gen-1* accelerometer interfaced with circuit; Differential sensitivity is equivalent to 163 mV/g

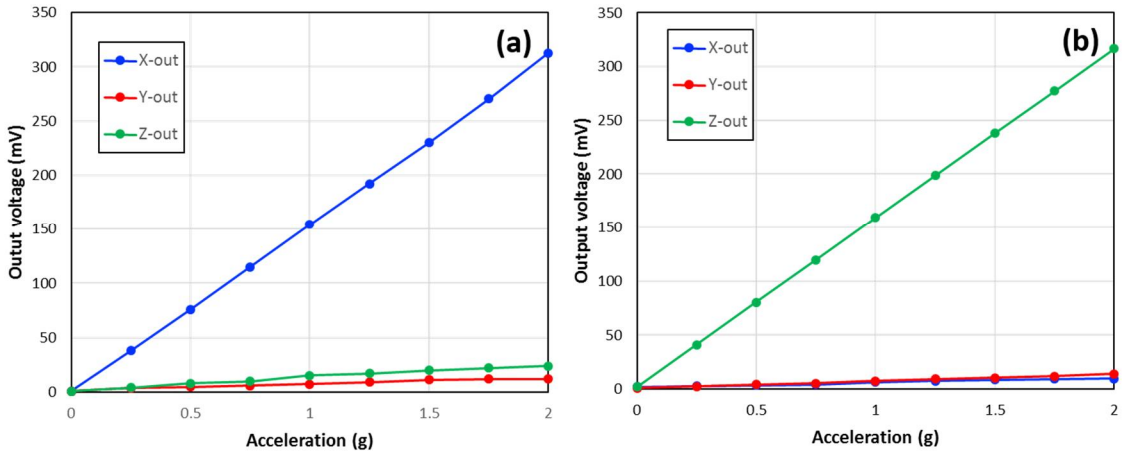


Figure 4. 46: Measured scale factor of *Gen-1* (a) in-plane and (b) out-of-plane accelerometer

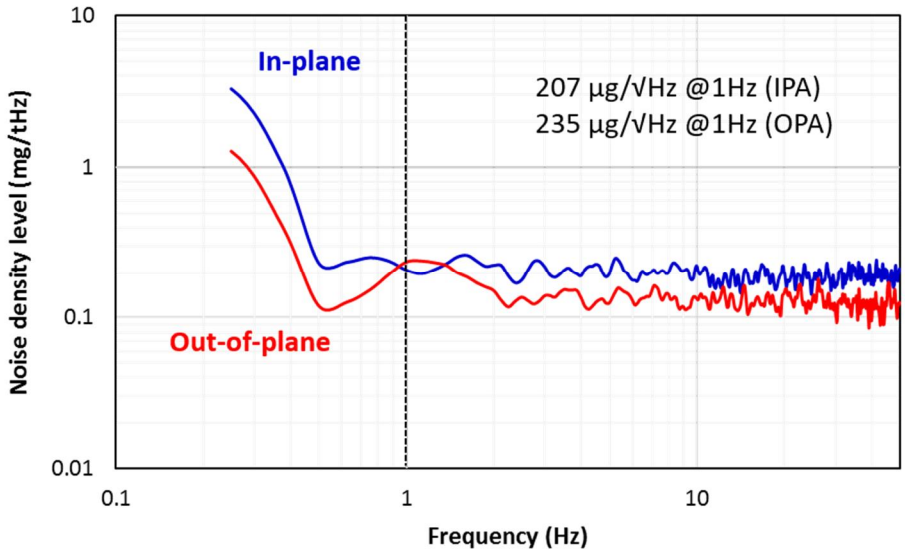


Figure 4. 47: Measured noise density level of Gen-1 accelerometer interfaced with readout circuit

The noise of the Gen-1 accelerometer was measured and plotted at Figure 4. 47, showing 207 µg√Hz and 235 µg√Hz at 1 Hz for in-plane and out-of-plane accelerometer respectively. The capacitive resolution level (ΔC_{min}) is calculated by dividing the output circuit noise with the capacitance-to-voltage gain and compared with readout circuit that was used to interface accelerometer on Table 4. 6**.** It is observed that even though the overall measured noise is higher than previous work, the noise performance of the presented readout circuit (i.e. capacitive resolution) is far better.

Table 4. 6: Comparison of capacitive resolution between other accelerometer circuit

	Measured output noise	Capacitive resolution (ΔC_{min})
Amini et al [30]	6 µg/√Hz	5 aF/√Hz
Adolvand et al [12]	200 ng/√Hz	7 aF/√Hz
MS3110 IC [62]	-	4 aF/√Hz
This work	**207 µg/√Hz**	**0.92 aF/√Hz**

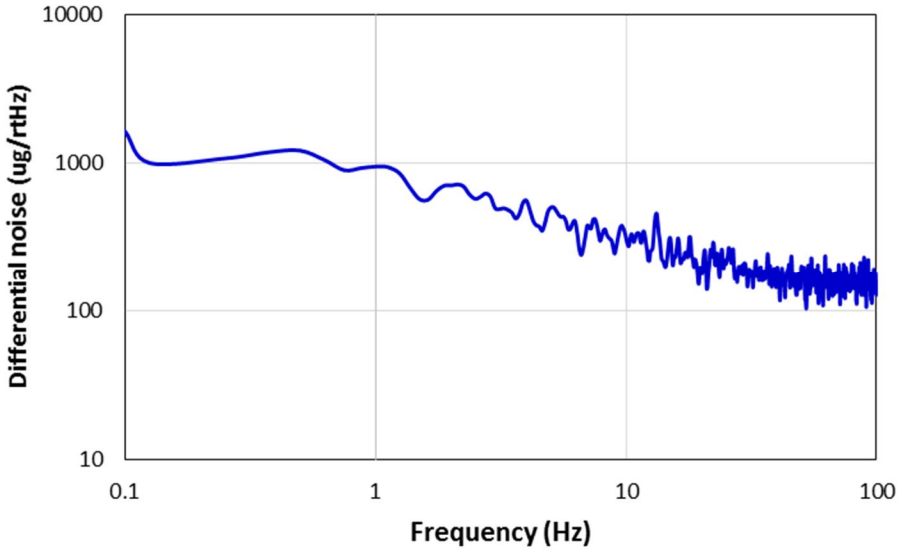


Figure 4. 48: Measured noise density level of *Gen-2* accelerometer interfaced with readout circuit

Unlike *Gen-1* design, *Gen-2* suffers from relatively large 1 Hz noise as shown in Figure 4. 48. This is a peculiar as the large noise is only observed at very low-frequency region (< 1 Hz). When the frequency increases (> 10Hz), the measured noise level reduces and becomes flat as similar to *Gen-1*. Further characterization process revealed that all of the *Gen-2* designs experienced a long settling behavior at internal summing node as shown in Figure 4. 49. This can be a serious problem for SC-amplifier, which uses CDS technique to cancel out the large 1/f noise and DC offset. The internal summing node is connected to the CDS capacitor, and if its voltage level does not settle within given clock period as

Figure 4. 48, there will be a deterioration on CDS operation, which results in portion of 1/f noise showing at the output. Initially large MEMS capacitance was suspected for such settling, but it was quickly dropped out as the *Gen-2* and *Gen-1* has similar static capacitance each other (3~4 pF).

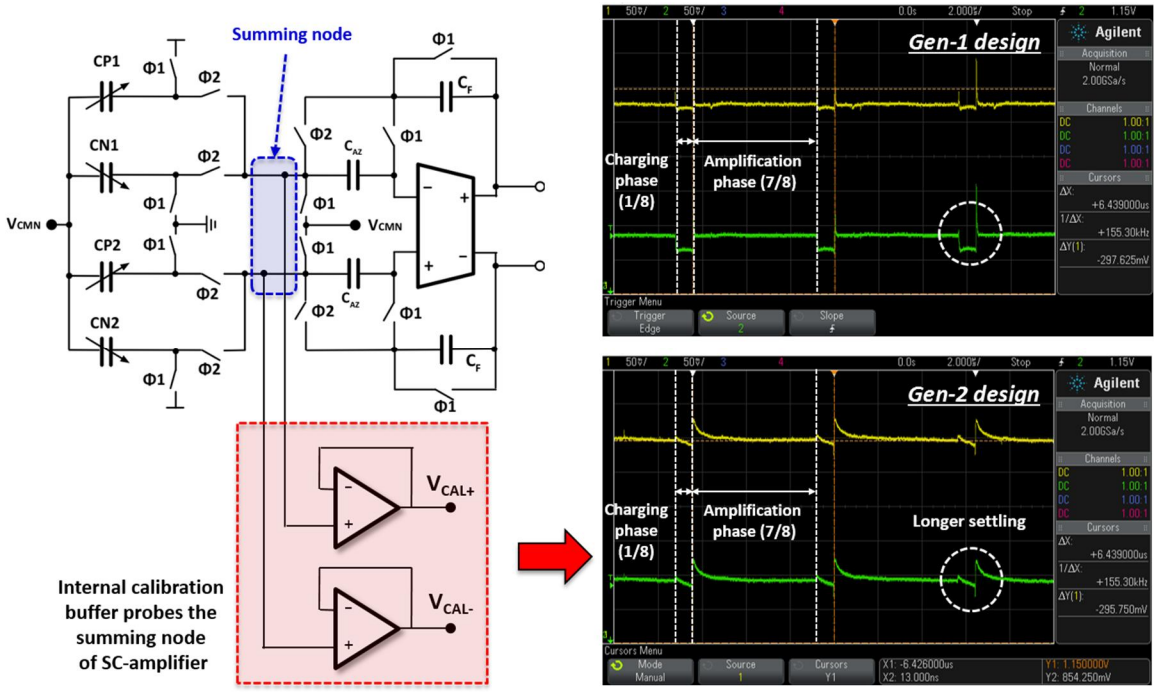


Figure 4. 49: (Left) Probing of internal summing node of SC-amplifier using calibration buffer (Right) Comparison of measured voltage level between *Gen-1* and *Gen-2* configuration

It turned out that the nitride plug, which is an added feature in *Gen-2* design as a protection barrier for supporting oxide layer [52], was the cause for such large noise. Silicon nitride material has a property that when sufficient electric field is applied, the electron tends to be injected into the dielectric layer and trapped inside. When interfaced with electronics, such characteristic prevents the switching voltage to be settled within given time period and thus harm the CDS operation. For full verification, the overshoot level of multiple accelerometer designs with different nitride plug area were compared and plotted as shown in with respect to its nitride plug area. As can be seen from Figure 4. 50,

the settling behavior becomes worse when nitride plug area is larger, indicating that there is a proportional relationship between amount of silicon nitride and noise increase.

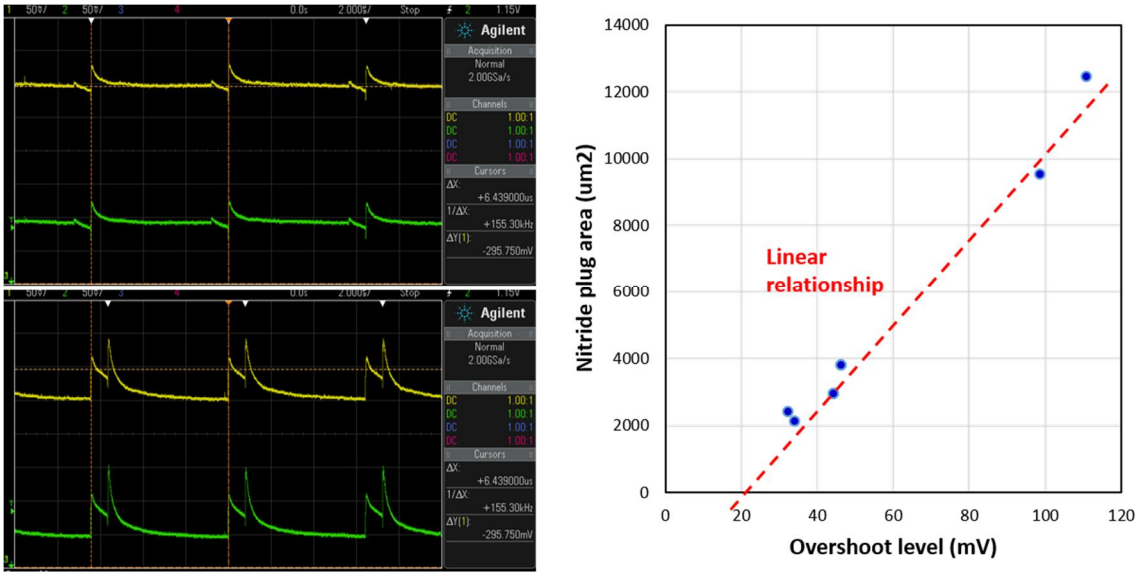


Figure 4. 50: (Left) Measured settling behavior on the summing node (Right) Measured overshoot with respect to nitride plug area

Lastly, the performance of temperature compensation block was characterized by inserting the evaluation board inside the temperature chamber and sweeping the temperature from -40 °C to 85 °C. Figure 4. 51(a) shows that by adjusting the temperature coefficient (TC) setting of the temperature sensor, the output level of the readout circuit changes accordingly. Some of the glitch behavior that is occurring during temperature sweep is thought to be environmental variation (bond-wire vibration) inside the chamber, and can be removed by proper packaging on the evaluation board. After the sweep, the overall bias variation over the entire temperature range was recorded, and by choosing minimum value, correct temperature coefficient setting was set. Figure 4. 51(b) compares the output of uncompensated accelerometer with that of compensated result. It is observed that by using the temperature compensation block, bias level variation of 5.8 g was suppressed to less than 300 mg level.

After the compensation, overall drift reduced from 400 mV to 120 mV, which is about 3-4 times of improvement.

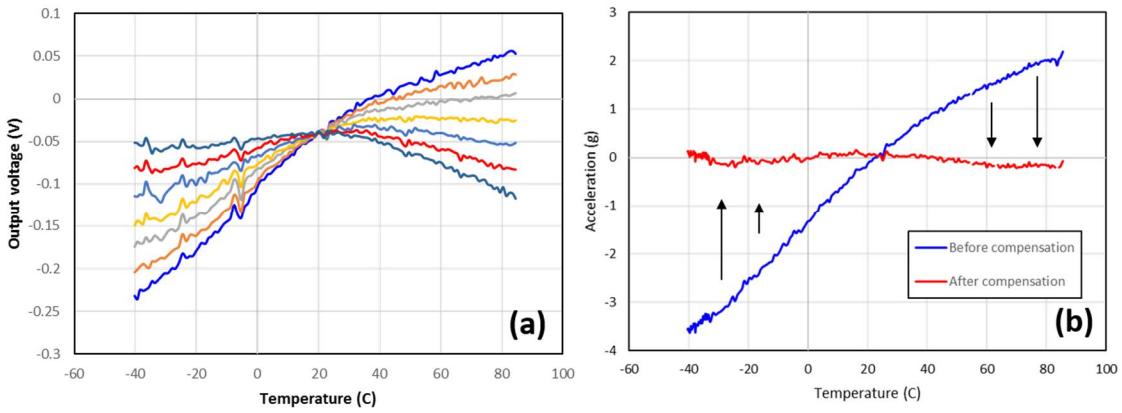


Figure 4. 51: Measured differential output of MEMS accelerometer interfaced with SC-amplifier under (a) different TC setting and (b) comparison between

One thing to note is that changes on the output level of MEMS accelerometer is not completely linear, and requires 3rd order correction using digital post-processing to achieve even less variation.

5. SINGLE PROOF-MASS TRI-AXIAL MEMS ACCELEROMETER

Although it is important to achieve precision performance for the accelerometer, in certain applications, such as IoTs (Internet of Things) or activity tracker, the device form-factor may have a greater impact on the specification requirement. To accommodate such needs, a number of commercial companies (Bosch, mCube) have recently released the accelerometer products focusing significantly on the miniaturization [9],[87]. These companies have met their objective by utilizing wafer level chip scale packaging (WLCSP) technology [10], which reduces their packaging size drastically. However, due to the complication of the assembly process, it raises the overall production cost and makes the sensor less enticed to the users.

To scale down the sensor size, designing a single-axis accelerometer may not be the best choice, because to create a sensor platform that can detect accelerations in all three-axis directions *(X/Y/Z-)*, multiple elements (two in-plane and one out-of-plane) are required. This would increase the entire area more than three times, and becomes huge obstacle when miniaturizing the device size. As an alternative, an accelerometer can be designed so that it can detect multiple axes of acceleration using single proof-mass microstructure. In this chapter, two different single proof-mass tri-axial accelerometer designs (pseudo-differential and fully differential) are presented and its operation will be discussed [88].

5.1. OPERATION PRINCIPLE OF PENDULUM ACCELEROMETER

Proposed single proof-mass accelerometer employs a pendulum-shaped mechanical structure to sense accelerations that are applied from multiple directions. Its simplified lumped-model diagram is shown on Figure 5. 1 (a), where the proof-mass *M* is

suspended by the mechanical spring *K*. The damping coefficient *D* is omitted for the simplicity. When the in-plane acceleration is applied, the proof-mass rotates with respect to the pivotal point (Figure 5. 1(b)) so that it results in in-plane (x_{in}) displacement. On the other hand, when the out-of-plane acceleration is applied, the proof-mass moves similar to the linear accelerometer (Figure 5. 1(c)), and results in out-of-plane (x_{out}) displacement.

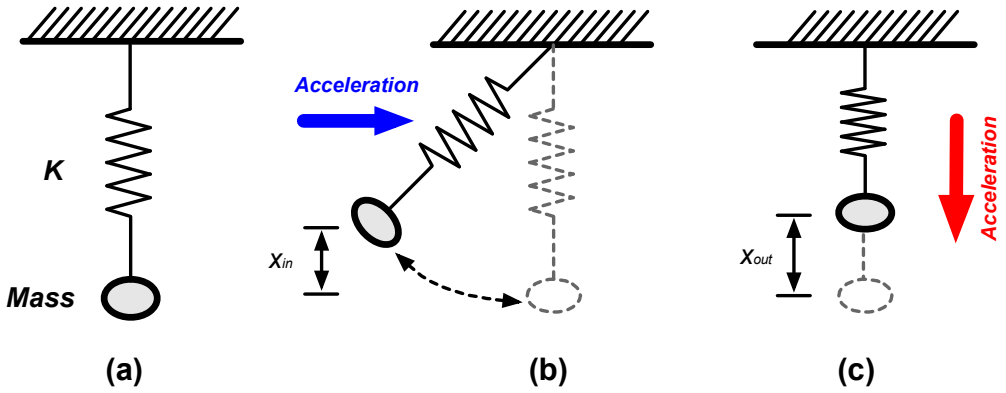


Figure 5. 1: (a) Simplified lumped model diagram of pendulum accelerometer and its movement under (b) in-plane and (c) out-of-plane acceleration

5.2. PSEUDO-DIFFERENTIAL PENDULUM ACCELEROMETER

5.2.1. SENSOR DESIGN

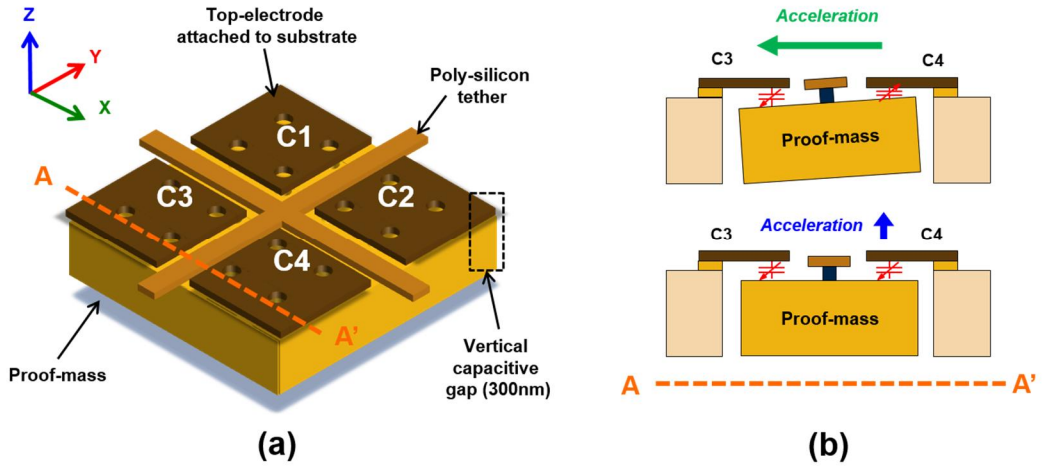


Figure 5. 2: (a) Schematic diagram of single-proof-mass accelerometer and (b) its cross-sectional movement in-plane (Top) and out-of-plane acceleration (Bottom)

Figure 5. 2(a) shows the overall schematic diagram of the proposed pendulum accelerometer [88]. The entire microstructure is consisted of single-crystalline-silicon (SCS) proof-mass suspended by the cross-shaped poly-silicon tethers. Four poly-silicon sense electrodes, C_1, C_2, C_3 and C_4 are placed on top of the proof-mass to detect out-of-plane displacement using changes on the capacitance. When the acceleration is applied on *x*- axis direction, the proof-mass tilted so that it increases the capacitance C_2/C_4 and decreases C_1/C_3 (Top Figure 5. 2(b)). The resulting differential capacitance change would be equivalent to $\Delta C_x=C_1-C_2+C_3-C_4$. Under *y*- axis acceleration, the resulting capacitance change would be $\Delta C_y=C_1+C_2-C_3-C_4$. Lastly, when the acceleration is applied on *z*- axis direction, all the sense capacitances *(C_1,C_2,C_3 and C_4)* would be either increasing or decreasing depending on the direction of proof-mass movement (Bottom Figure 5. 2(b)). By employing a reference capacitor C_0 that is same as sense capacitances *(C1,C2,C3 and C4)*, the change would be $\Delta C_z=C_1+C_2+C_3+C_4-4C_0$. As differential capacitance sensing is used for the output of each channel, low cross-axis sensitivity performance can be attained.

The cross-shaped poly-silicon tether behaves differently depending on the axis of applied acceleration. When the acceleration is exerted along the in-plane direction (*x*-/*y*-axis), the tether is considered as two torsional beams combined with two clamped-pinned beams [89]. On this configuration, the proof-mass would rotate based on the beam stiffness, which are expressed as equation (5-1) and (5-2), where *G* stands for the shear modulus of the silicon, α represents the correction factor depending on the aspect ratio of the beam.

$$K_{\theta.torsion}=\frac{4G\alpha h_t w_t^3}{l_t},\ K_{\theta.clamped-pinned}=\frac{4}{3}\frac{E}{l_t}w_t h_t^3 \qquad (5\text{-}1)$$

$$K_{in-plane} = 2 \cdot (K_{\theta.torsion} + K_{\theta.clamped-pinned}) \qquad (5\text{-}2)$$

The tilted angle θ of the proof-mass under in-plane acceleration is expressed as equation (5-3) using the Newton's second law of the rotational inertia [89]. The differential capacitance change between the top sensing electrodes and the proof-mass can be derived as equation (5-4), where l_m represents the length of the top electrode, a as distance between center of mass and sensing area, and g_0 as initial gap size respectively.

$$\theta = \frac{\tau_{ext}}{K_{in-plane}} = \frac{M \cdot r}{K_{in-plane}} \overrightarrow{a_{ext}} \qquad (5\text{-}3)$$

$$\Delta C = C_+ - C_- = \varepsilon_0 l_m \int_a^{a+l_m} \frac{1}{g_0 - x\tan\theta} dx - \varepsilon_0 l_m \int_a^{a+l_m} \frac{1}{g_0 + x\tan\theta} dx \qquad (5\text{-}4)$$

When out-of-plane acceleration is applied, cross-shaped tether is considered as parallel connection between four silicon beams, which stiffness is represented as equation (5-5). E indicates the Young's modulus of silicon, w_t as width of the poly-silicon tether, h_t as thickness, and l_t as length of the poly-silicon tether.

$$K_{out-of-plane} = 4 \cdot K_{beam} = 4EW_t \left(\frac{h_t}{l_t}\right)^3 \qquad (5\text{-}5)$$

The out-of-plane response can be interpreted as a translational movement of the proof-mass, which displacement is expressed as equation (5-6).

$$x_{out-of-plane} = \frac{M}{K_{out-of-plane}} \overrightarrow{a_{ext}} \qquad (5\text{-}6)$$

The poly-silicon tether needs to be designed in a way so that similar performance can be achieved for all three axes. Extensive FEM simulation using ANSYS program was performed to extract various system parameters such as scale factor, pull-in voltage, and squeezed film damping coefficient. Figure 5. 3 and Figure 5. 4 shows the electrostatic and the squeezed film damping simulation result when the acceleration is applied in both in-plane and out-of-plane directions. Table 5. 1 summarizes the device geometry and simulated performances of the pseudo-differential accelerometer design.

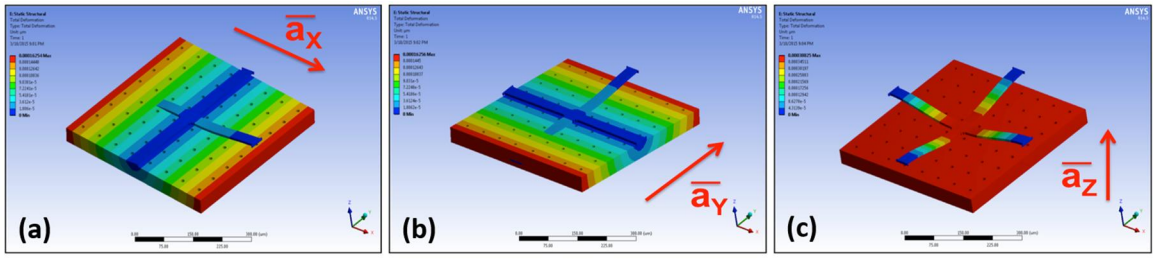


Figure 5. 3: Electrostatic simulation of pseudo-differential accelerometer under *x*-, *y*- and *z*-axis of acceleration

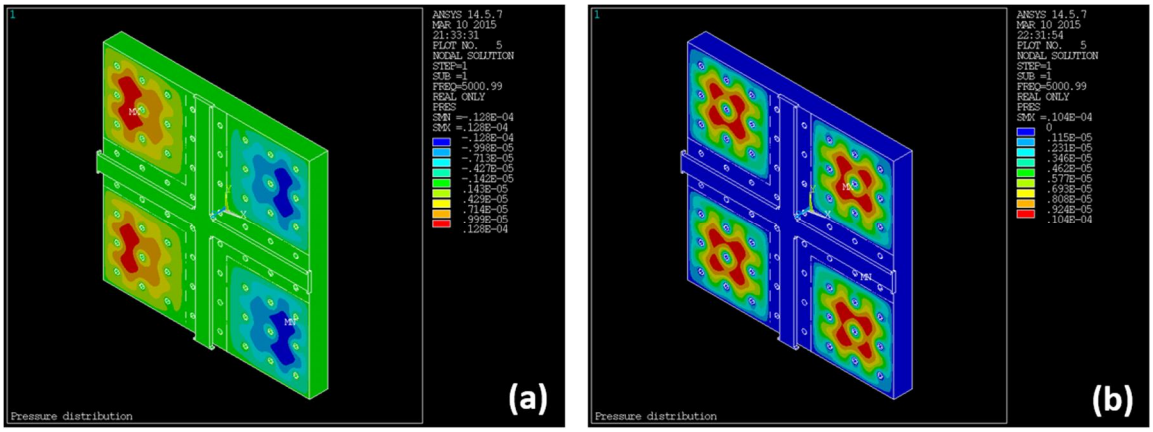


Figure 5. 4: Squeezed-film-damping simulation of pseudo-differential accelerometer under (a) in-plane and (b) out-of-plane acceleration

Table 5. 1: Simulated performance summary of pseudo-differential accelerometer

Parameter	In-plane movement	Out-of-plane movement
Proof-mass size	450 μm × 450 μm × 40 μm	
Capacitive gap size	300 nm	
Resonance frequency	22.527 kHz	25.429 kHz
Capacitive sensitivity	2.5 fF/g	7.5 fF/g
Linear range	± 35 g	± 8 g
Brownian noise	35.96 μg/√Hz	38.2 μg/√Hz
Pull-in voltage	1.5 V	2.2 V

5.2.2. FABRICATION AND MEASUREMENT RESULT

Proposed pseudo-differential accelerometer is fabricated using HARPSS process [39]-[40] on a 40 μm thick silicon-on-insulator (SOI) wafer. It is wafer-level vacuum packaged using a same process as the single-axis accelerometer that is mentioned in prior section. Figure 5. 5 shows the SEM microphotograph of the fabricated device, which clearly shows the 300 nm capacitive gap between the proof-mass and the top-poly electrode. The functionality of the fabricated device is first verified by measuring its resonance response. The MEMS accelerometer was placed inside the pressure-controlled chamber and connected with vector network analyzer. Two sense electrodes are tied to the excitation ports to constantly actuate the proof-mass using sinusoidal voltage. The proof-mass movement is then translated into a current generated from the other two sense electrodes on the opposite side. During measurement, the pressure level inside the chamber was brought down to a level (<100 mTorr) where the air-damping is negligible so that the resonance response can be observed. Figure 5. 6 shows that the resonance peaks are measured at 24 kHz for *x/y*- axis and 28 kHz for *z*- axis movement, which is in good agreement with the simulation results.

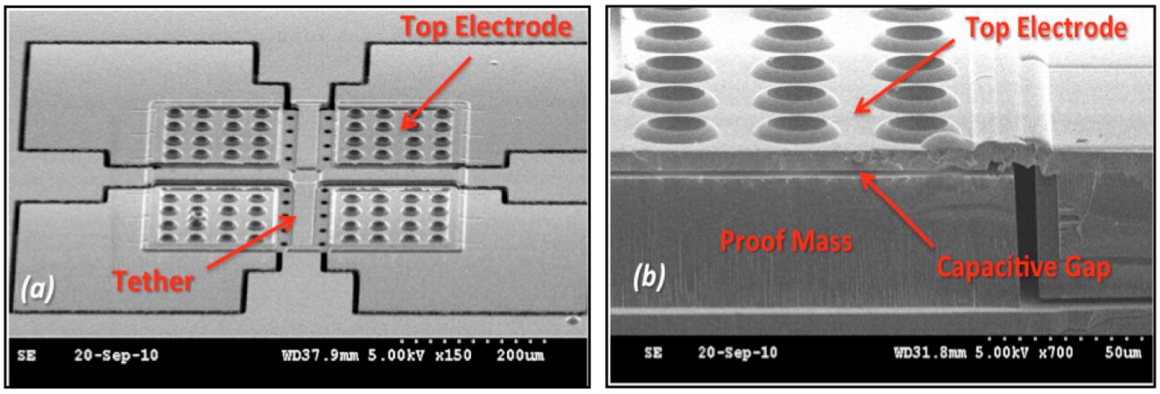


Figure 5. 5: SEM photo of fabricated (a) accelerometer and (b) its cross-section view; capacitive gap between proof-mass and top electrode is 300 nm

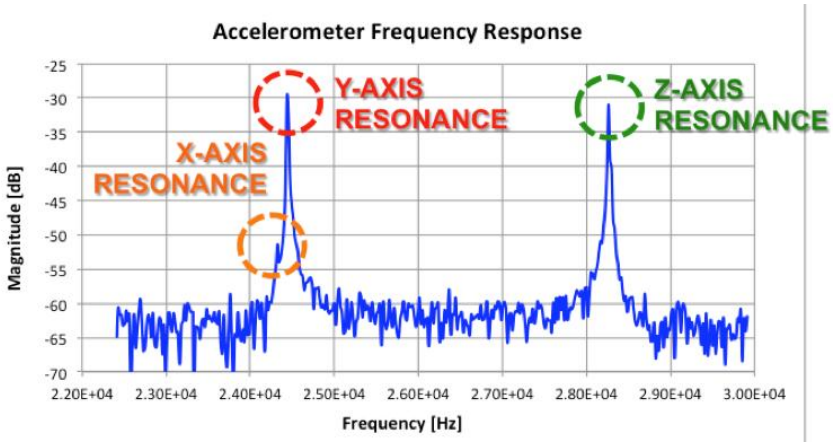


Figure 5. 6: Resonance response of accelerometer when ambient pressure level is 100mTorr

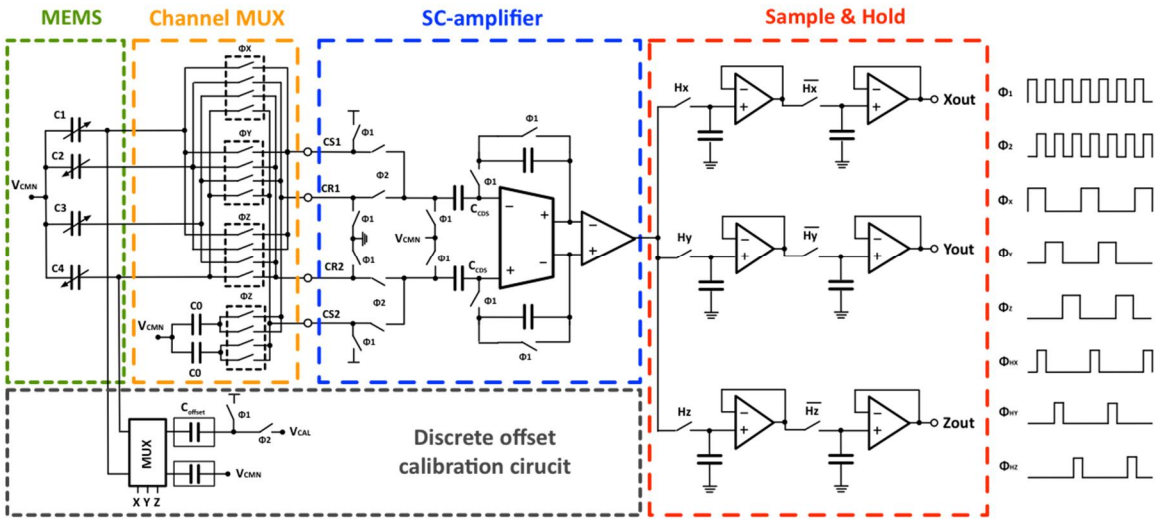


Figure 5. 7: Schematic connection between MEMS Accelerometer and interface circuit; Channel mux at the input connects the MEMS capacitor in right axial configuration

After verifying its functionality, the overall performance was characterized by interfacing MEMS sensor with readout ASIC, which schematic is shown at Figure 5. 7. The circuit has channel multiplexer block at its input so that proper MEMS electrodes are connected to the SC-amplifier with correct manner when each channel is enabled. For example, when *x*- axis is enabled, MEMS capacitance C_1, C_2, C_3 and C_4 is connected to SC-amplifier inputs, C_{S1}, C_{R1}, C_{R2}, and C_{S2} accordingly. Under such configuration, only the capacitance change under *x*- axis acceleration $(C_x=C_1-C_2+C_3-C_4)$ gets amplified, but the capacitance changes at other axial acceleration (C_y and C_z) are considered as common-mode variation and will be canceled out (Differential sensing). The amplified output is then demultiplexed into separate channels using sample and hold block.

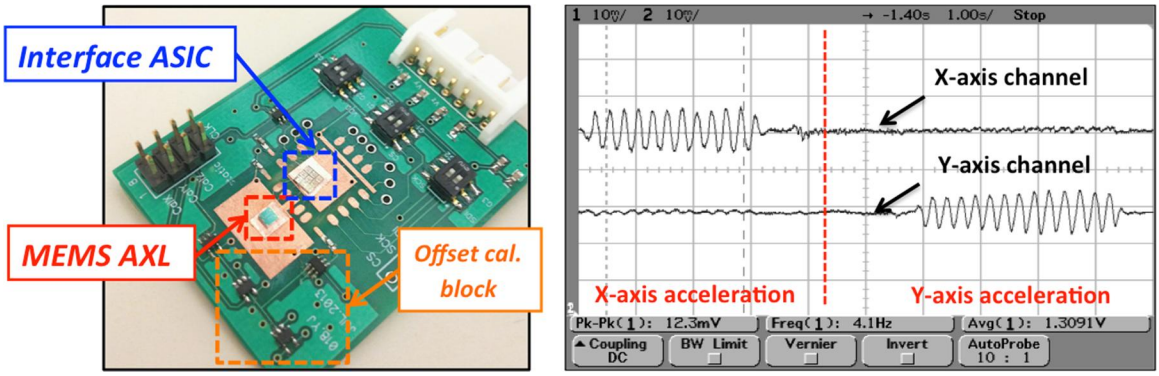


Figure 5. 8: (Left) Photo of evaluation board; MEMS AXL and the interface circuit is connected using wire-bond. (Right) Output of the interface circuit under acceleration

Figure 5. 8 shows the output of the proposed pseudo-differential accelerometer when sinusoidal acceleration is applied on each *x*- and *y*- axis separately. It is important to note that each channel output *(x-/y-)* only responds with the corresponding accelerations. That is, the *x*- channel only responds to *x*- axis acceleration, but not with the acceleration on *y*- axis. Such behavior proves good cross-axis rejection of the sensor. Measured scale factor of the device is plotted at Figure 5. 9, where in-plane acceleration is 5.1 mV/g and

out-of-plane acceleration is 10.9 mV/g respectively. The cross-axis sensitivity is between 1 ~ 3 %, which is mostly due to the misalignment error between evaluation board and the shaker table. The measured output noise of the system (MEMS + ASIC) is in the order of 3 to 6 mg/√Hz, with the bias drift of 20 mg (Figure 5. 10). Large noise is attributed due to the readout electronics (Figure 5. 7). Through careful optimization on the readout electronics, the overall response can be limited by the mechanical noise, which is designed to be around 30 to 40 µg/√Hz at 10 Torr pressure level. Table 5. 2 summarizes the overall performance of the proposed pseudo-differential accelerometer.

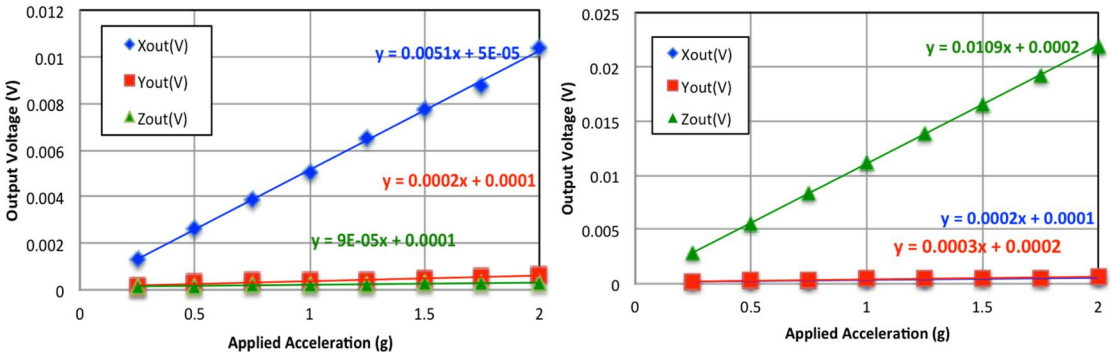


Figure 5. 9: Measured scale factor of pseudo-differential sensor under in-plane (left) and out-of-plane acceleration (right)

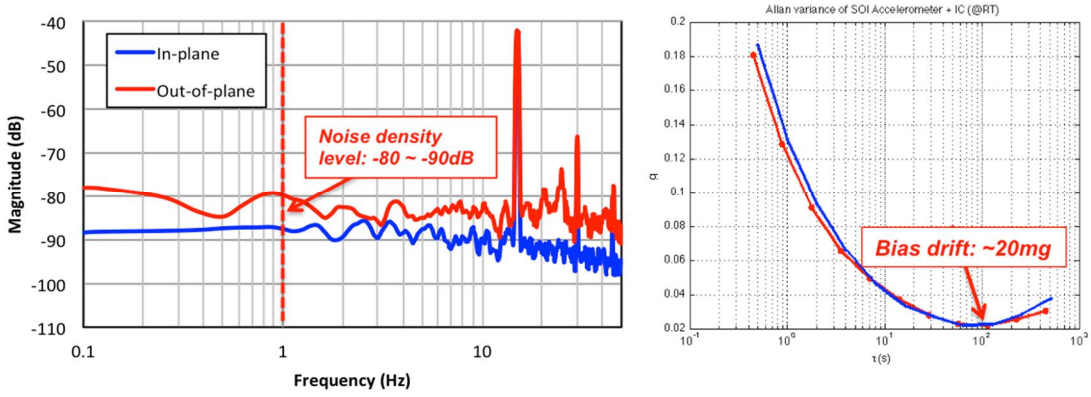


Figure 5. 10: Measured noise density level of -90 dBV$_{rms}$ (left) and Allan variance plot of tri-axial accelerometer (right)

Table 5. 2: Measurement summary of pseudo-differential accelerometer

Parameter	In-plane response	Out-of-plane
Resonance frequency	24 kHz	28 kHz
Sensitivity	5 mV/g	10.9 mV/g
Linear range	±12 g	±6 g
Cross-axis sensitivity	3% (x/y), 1.1% (z)	1% (x), 1.8% (y)
Noise level	6 mg/√Hz	3mg/√Hz
Bias drift	~ 20 mg	

5.3 FULLY-DIFFERENTIAL PENDULUM ACCELEROMETER

5.3.1 SENSOR DESIGN

One of the major issue in prior pseudo-differential accelerometer is that it does not employs differential capacitance sensing for the out-of-plane acceleration sensing. This leads to increase in the noise level, and requires large reference capacitor arrays *(C_0)* to be integrated into the readout circuit. To address such problems, a fully-differential accelerometer, which schematic diagram is shown on Figure 5. 11 is proposed. Presented design has 8 poly-silicon electrodes, where C_1, C_2, C_3, and C_4 are tied to the silicon substrate (inner electrodes), whereas C_5, C_6, C_7 and C_8 is attached to the proof-mass (outer electrodes). Each electrode has identical sensing area (300 nm gap) to minimize capacitance mismatches with other electrodes. During operation, the inner electrodes (C_1~C_4) are remain fixed to the silicon substrate, but the outer electrodes (C_5~C_8) moves with the proof-mass, making the device to have differential capacitance change with respect to all three-axis of acceleration. As shown in Figure 5. 11(b), when the acceleration is applied in out-of-plane direction, the proof-mass moves upward, and the capacitance at

inner electrode (C_1~C_4) increases as the gap size gets decreased. On the other hand, the outer electrode (C_5~C_8) moves with the proof-mass and decreased due to increased gap size. The resulting differential capacitance change would be $C_z=C_1+C_2+C_3+C_4-C_5-C_6-C_7-C_8$. Similar behavior is observed for *x*- and *y*-axis acceleration as well. The capacitance change at the inner electrode will be as same as pseudo-differential accelerometer operation, but for the outer electrode, the change will be opposite as the electrodes moves with the proof-mass. Therefore, the capacitance change at the *x*- axis will be $\Delta C_x=C_1+C_2-C_3-C_4-C_5-C_6+C_7+C_8$, and $\Delta C_y=C_1-C_2+C_3-C_4-C_5+C_6-C_7+C_8$ for *y*- axis acceleration, respectively.

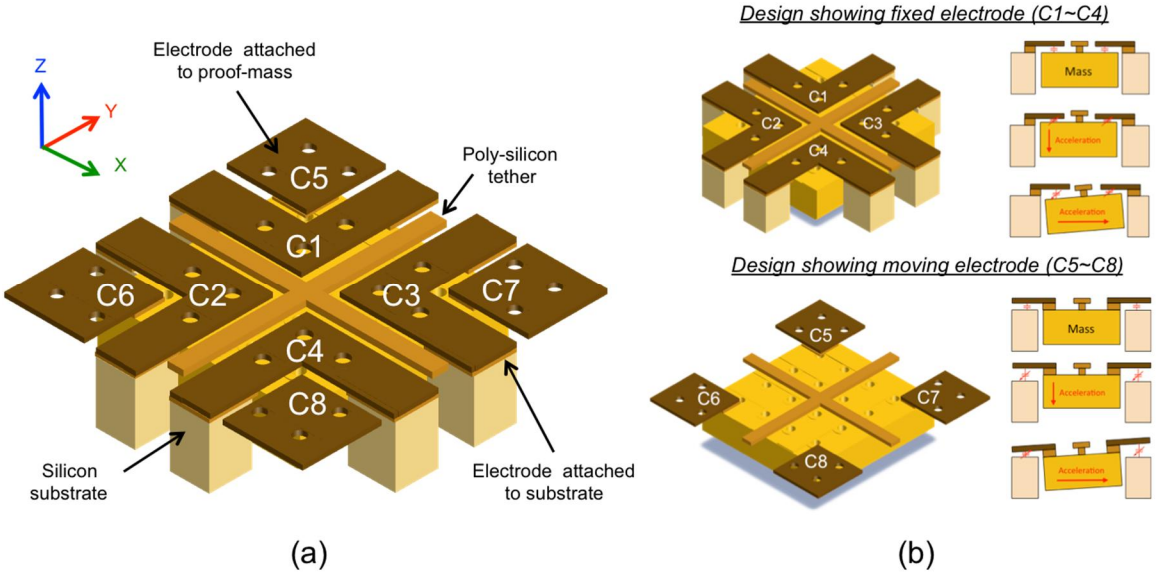


Figure 5. 11: (a) Schematic diagram of fully differential accelerometer and (b) its operation under in-plane and out-of-plane acceleration;

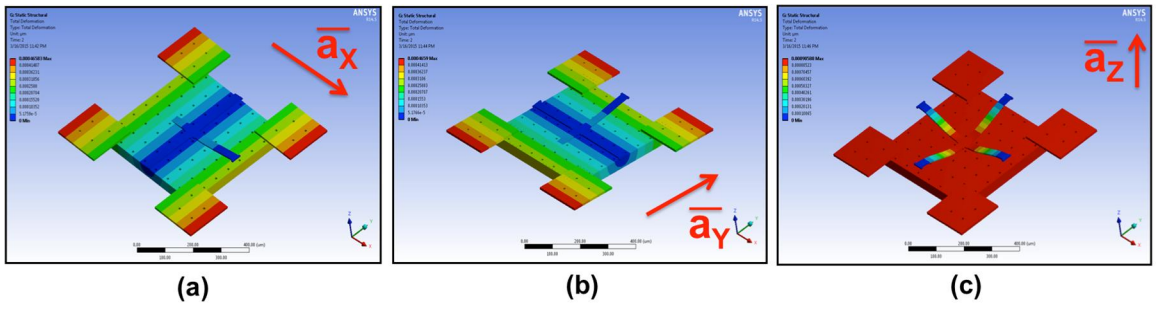


Figure 5. 12: Electrostatic simulation of fully differential accelerometer under (a) x-axis, (b) y-axis and (c) z-axis acceleration

Figure 5. 12 shows the electrostatic simulation of the fully differential sensor under all three-axis of acceleration *(x/y/z)*. The in-plane scale factor is 5.2 fF/g and out-of-plane scale factor is 16.4 fF/g, which is far higher than that of pseudo-differential design. Figure 5. 13 shows the squeezed film damping simulation of the sensor under 10 Torr pressure level. Other design parameter and simulation result are summarized on Table 5. 3.

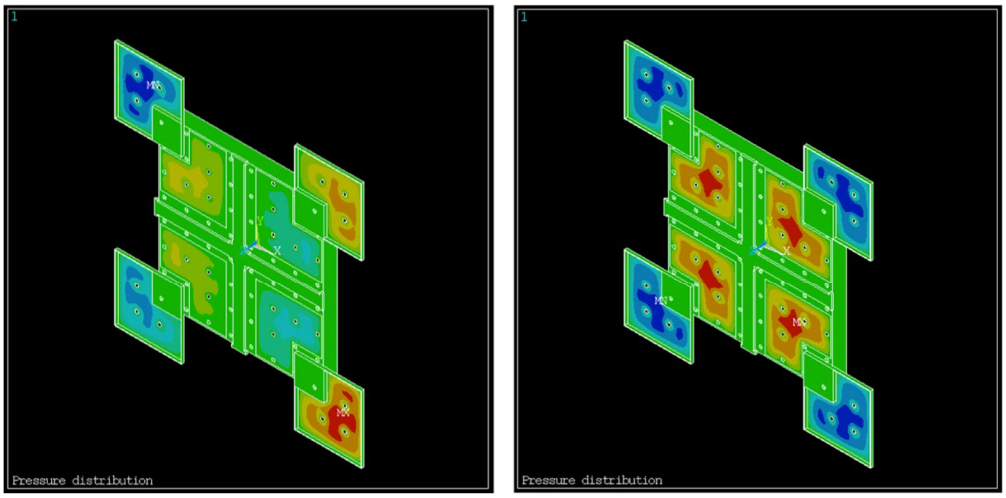


Figure 5. 13: Squeezed film-damping simulation of fully differential accelerometer under (a) in-plane and (b) out-of-plane movement

Table 5. 3: Design simulation result summary of fully differential accelerometer

Parameter	**In-plane**	**Out-of-plane**
Proof-mass size	450 µm x 450 µm x 40 µm	
Capacitive gap size	300 nm	
Sense electrode capacitance	750 fF	
Resonance frequency	12.8 kHz	17. 5 kHz
Capacitive sensitivity	5.2 fF/g	16.4 fF/g
BNEA	12.8 µg/√Hz	30.7 µg/√Hz
CNEA	96 µg/√Hz	30 µg/√Hz
Pull-in voltage	1.5 V	

5.3.2. FABRICATION AND MEASUREMENT RESULT

Fully-differential accelerometer is implemented using HARPSS process [39]-[40] and consecutively wafer-level vacuum packaged (1~10 Torr). Figure 5. 14 shows the SEM microphotograph of fabricated accelerometer, which has similar shape as Figure 5. 5 except for the poly-silicon electrodes attached to the proof-mass. Fabricated sensor is interfaced with the readout circuit that has on-chip offset calibration block (Figure 5. 15), and attached to the shaker table to apply acceleration in all three-axis. Measured scale factor show 36.75 mV/g for x-axis, 43.31mV/g for y-axis, and 26.9mV/g for z-axis. Considering the circuit gain is 11.72 mV/fF for *x*- and *y*- axis channel and 2.93 mV/g for *z*- axis channel, capacitive sensitivity of the MEMS accelerometer can be back-calculated as 3.13 fF/g (*x*- axis), 3.69 fF/g (*y*- axis) and 9.18 fF/g (*z*- axis), which is similar to the simulation result. Measured cross-axis sensitivity is 3 ~ 5 %, which is a bit higher than the pseudo-differential accelerometer. Even though misalignment between sensor orientation and the axis of acceleration may have deteriorated the cross-axis performance, further investigation is required to verify the root cause. Measured noise density level is 38.97 μVrms/√Hz for *x*-axis and 39.78 μVrms/√Hz for *z*- axis channel, which is 2 to 3 times better than previous pseudo-differential design. The measured bias drift is 1 mg. Table 5. 4 summarizes down the measurement result of the fully-differential accelerometer interfaced with readout ASIC. Utilization of fully differential capacitance sensing and optimized circuitry enhances the system performance more than 2~ 3 time compared to that of previous pseudo-differential design.

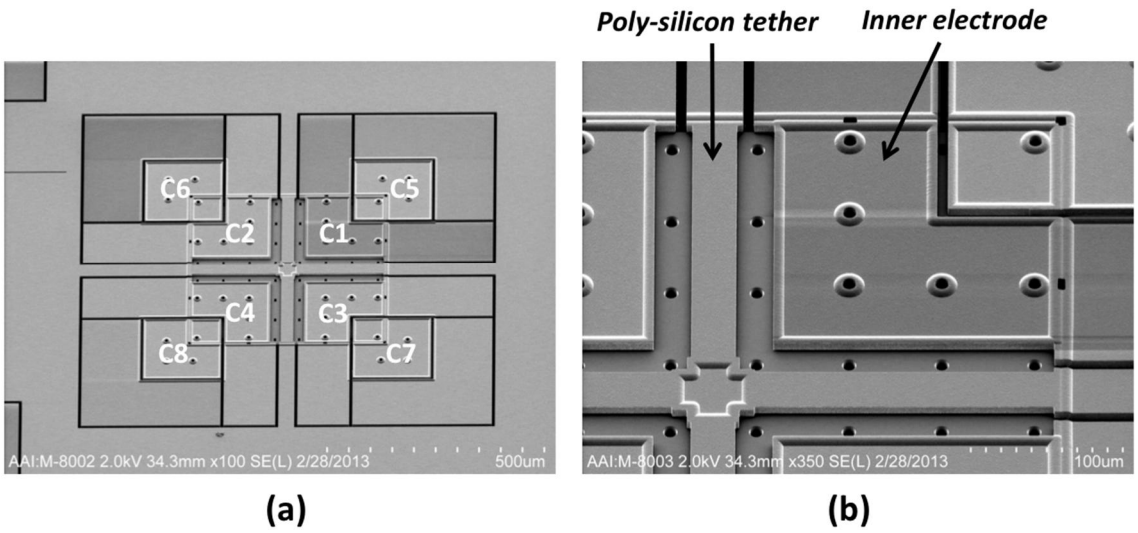


Figure 5. 14: SEM photo of (a) fully differential accelerometer and (b) closed-up view on cross-shaped poly-silicon tether region

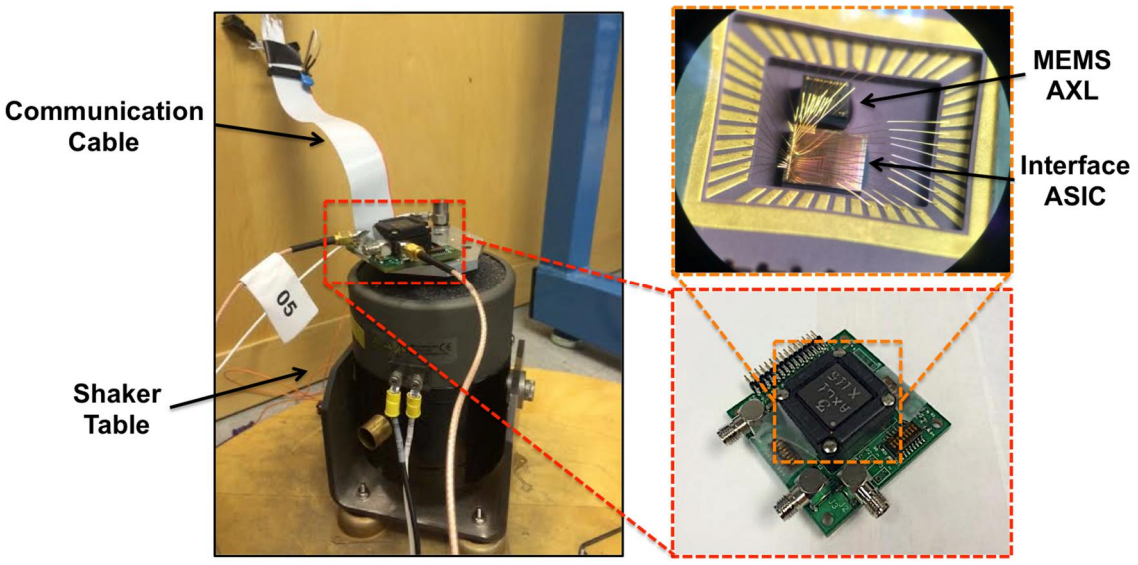


Figure 5. 15: Photo of measurement setup (Left), evaluation board (Bottom-right), and inside the ceramic package (Top-right)

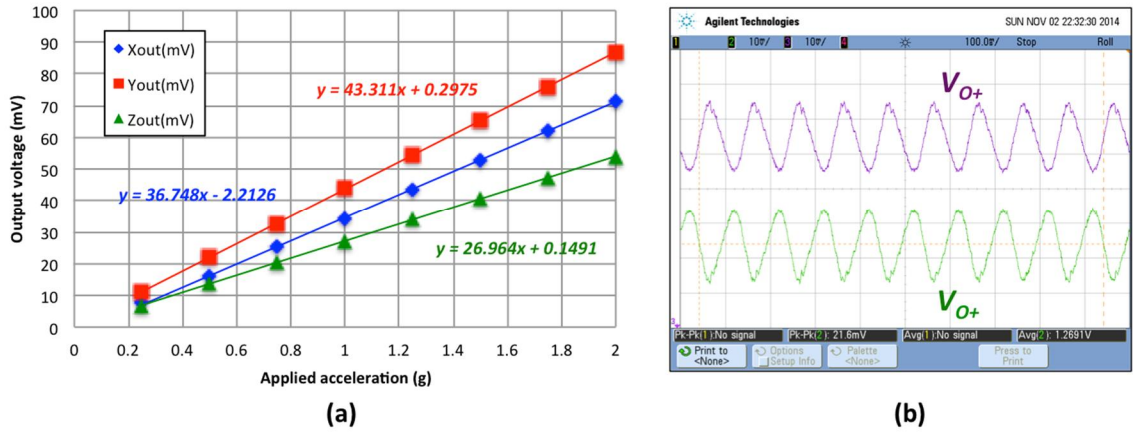


Figure 5. 16: (a) Output response of accelerometer under sinusoidal acceleration (b) Measured scale factor for all three-axis of acceleration

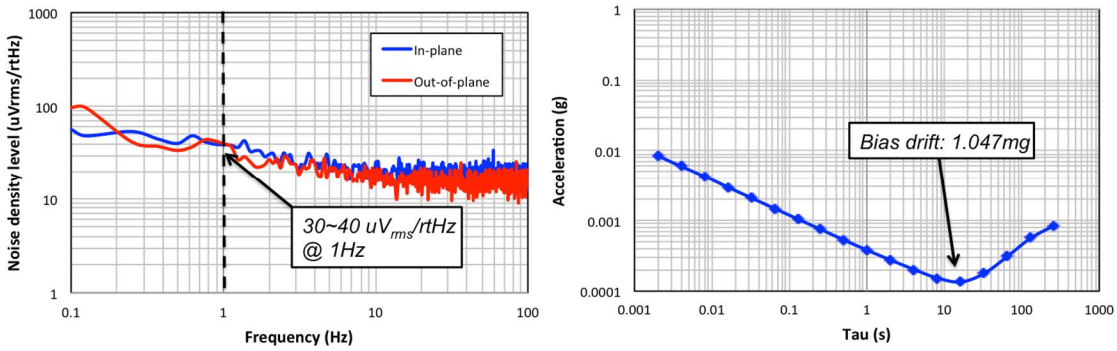


Figure 5. 17: (a) Measured noise and (b) bias drift of fully-differential accelerometer

Table 5. 4: Measurement summary of fully differential accelerometer interfaced with ASIC

Parameter	In-plane response	Out-of-plane response
Proof-mass size	450 µm x 450 µm x 40 µm	
Capacitive gap size	300 nm	
Sensitivity	36.748 mV/g (*x-axis*) 43.311 mV/g (*y-axis*)	26.964 mV/g (*z-axis*)
Cross-axis sensitivity	3.65 %	4.98%
Noise density level	38.97 µV/Hz (=987 µg/√Hz)	39.78 µV/√Hz (=1.489 mg/√Hz)
Bias drift	1.047 mg	

6. CONCLUSIONS AND FUTURE WORK

6.1 CONTRIBUTIONS

Presented dissertation has investigated the design and characterization of tri-axial MEMS capacitive accelerometer, which utilizes high aspect ratio sub-micron sensing gap to achieve extended operational bandwidth while maintaining low-noise performance. Fabricated accelerometer is interfaced with signal-conditioning readout ASIC to suppress any non-ideal capacitive mismatch of the device, and to attain low-noise output signal. Number of various measurements were conducted to characterize its performance and to prove feasibility of the proposed accelerometer for newly-emerging applications, such as wearables, IoTs (Internet of Things). The major contributions of the dissertation are summarized as below.

I. Tri-axial μ-g MEMS accelerometers with nano-gap
    A. Design and characterization of capacitive MEMS accelerometer utilizing high aspect ratio (>100:1) sub-micron gap (< 300 nm) to achieve wide-bandwidth, low-noise performance. Such characteristic is enabled by increased electromechanical coupling provided by the narrow gap structure.
    B. Demonstration of first open-loop capacitive accelerometer operating under low-pressure environment (1~10 Torr) without any instability issue. Both sensing and damping electrodes implemented with nano-gap structure provides additional squeezed-film-damping to stabilize quasi-static accelerometer operation in low-pressure level.

C. A novel damping electrode structure design utilizing both lateral and vertical nano-capacitive gap to achieve improved stability without sacrificing pull-in voltage limit on design.

D. Demonstration of first open-loop capacitive MEMS accelerometer, which measured operational bandwidth is higher than 8.5 kHz, and the noise density level close to 100 μg/√Hz. This was not possible using conventional MEMS accelerometer design.

E. Shock-stop implementation for nano-gap accelerometers using sloped electrode design to attain improved device robustness again high-g acceleration level

F. Hinge-shaped out-of-plane accelerometer with improved fabrication yield

II. Low-noise & low offset SC signal-conditioning IC

A. In-depth analysis to determine major source for accelerometer circuit noise *(CNEA)* and implemented the circuit to suppress such noise contributors.

B. Suppressing non-ideal capacitive mismatch and temperature variation on MEMS accelerometer using time-averaged charge-tuning technique, which is capable of providing fine resolution as well as wide calibration range

C. Detailed system level characterization of MEMS+ASIC

III. Single-chip Inertial Measurement Unit (IMU)

A. Paved the way toward the single-chip inertial measurement unit (IMU) implementation by integrating presented capacitive MEMS accelerometers with different resonant devices (Gyroscopes, Timing resonator) in common low-pressure level environment (1~10 Torr).

6.2. FUTURE WORKS

Proposed MEMS accelerometer utilizing high aspect ratio sub-micron sensing gap have validated the design as a promising candidate for newly-emerging applications. This also opens up the new possibilities of the application getting expanded toward even greater area, which was not possible using conventional accelerometer design methodology.

The contact microphone captures the vibration of audio waves through the contact with solid objects [92]. It has been often used in various applications such as electronic stethoscope, musical instrument, or vibration sensing. Recently, there has been a growing interest on the use of contact microphone to detect the joint sounds to diagnose the leg injury of a patient [93]-[94]. However, using conventional contact microphone is challenging due to its large form-factor and expensive cost [95]. If existing design, which is usually made using piezoelectric material, can be replaced with MEMS accelerometer, it would be a significant advantage for its miniaturized size and low fabrication cost. The feasibility of measuring acoustic sounds using MEMS accelerometer has already been studied previously [96], however, several limitations does exist due to the large noise (> 200 μg/rtHz) and narrow operational bandwidth (~5 kHz).

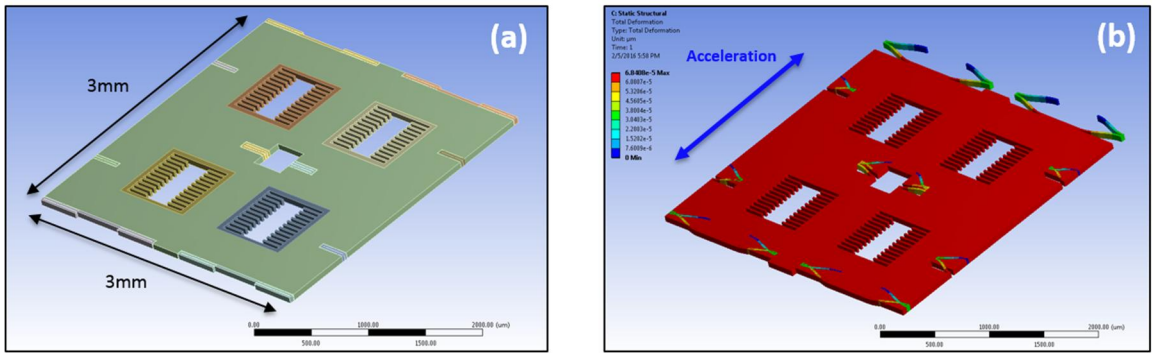


Figure 6. 1: (a) Schematic diagram of proposed micro-g contact microphone and (b) its movement under 1g acceleration

Presented accelerometer design can be effectively used to address the issues, as it has already demonstrated resonant frequency that is several times higher (~15 kHz) than that of conventional designs (2~5 kHz), while maintaining low-noise performance (~100 μg/√Hz). Considering the accelerometer is a 2nd order system, which operational bandwidth is determined based on the device resonant frequency, such characteristic enables achieving far wider operational bandwidth compared to the conventional product. To assess feasibility, preliminary design has been simulated as shown on Figure 6. 1. The sensing gap size is 190 nm with silicon thickness of 60 μm. FEM analysis shows that the design has resonance frequency of 19.165 kHz and scale factor of 202.7 fF/g, which is translated into total noise density level of 6.52 μg/√Hz.

The angular accelerometer is a device that detects the angular accelerations ($^o/sec^2$) applied on the microstructure. It is consisted of proof-mass that is connected to a mechanical spring that responds to external rotation in different axis *(Yaw-/Roll-/Pitch-)*. Thanks to inherent quasi-static operation, the angular accelerometer can detect rotation using orders of lesser power compared to gyroscope. However, the usage has been limited to specific applications, such as HDD (Hard-disk drive) monitoring [97][98], due to poor scale factor noise performance.

The presented design methodology for MEMS linear accelerometer, which utilizes high aspect ratio sub-micron sensing gap, can be effectively employed to create a MEMS angular accelerometer with improved performance. As the capacitive sensitivity is a strong function of the electrode geometry, by scaling down its sensing gap size, the scale factor can be improved significantly without relying on a large proof-mass. To validate the feasibility of implementing angular accelerometer with narrow sensing gap, a dual-axis

single-proof-mass angular accelerometer has been demonstrated as shown in Figure 6. 2 [99]. A dumbbell-shaped proof-mass is centrally anchored via two mechanical tethers. When the angular acceleration is applied along the yaw-axis, the mechanical tether behaves as a bending beam and the proof-mass rotates within in-plane direction. On the other hand, when the angular acceleration is applied along the pitch-axis, the mechanical tether acts as a torsional hinge and the proof-mass rotates at an out-of-plane direction. The differential capacitance change under yaw-axis angular acceleration is equivalent to $\Delta C_{yaw}=(C1-C2)-(C3-C4)$, and pitch-axis is $\Delta C_{pitch}=(C1-C2)+(C3-C4)$.

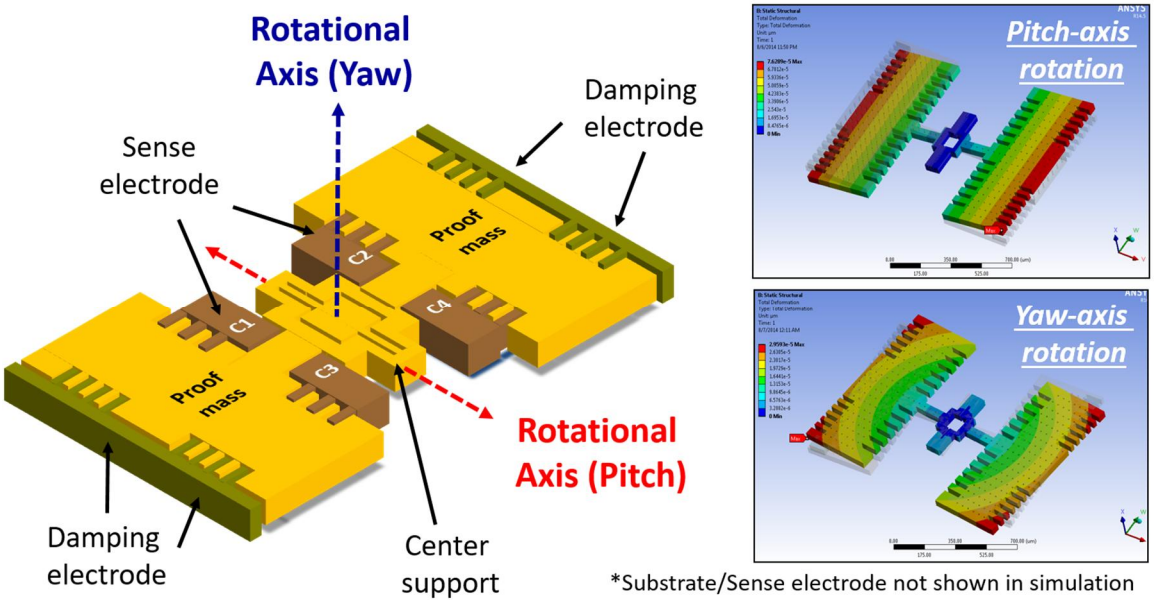


Figure 6. 2: Schematic diagram of dual-axis angular accelerometer and its movement under different axes of angular acceleration [99]

Proposed design can be further revised to detect angular accelerations that are applied on all three-axis direction *(Yaw-/Roll-/Pitch-)*. Further optimization is required for the device to achieve improved capacitive sensitivity and the noise performance. Such design can be a promising candidate for application that requires rotation rate sensing using far smaller power consumption compared to conventional gyroscopes.

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